TOSHIBA

FILE NO. 336-9707

# TECHNICAL TRAINING MANUAL

# 3 LCD DATA PROJECTOR

# *TLP511U*
# *TLP510U*
# *TLP511E*
# *TLP510E*

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# 1. MAIN POWER SUPPLY CIRCUIT

## 1-1. Description

This power supply boosts up at boost-up-converter just after bridge-rectifying AC input voltage, supplies the voltage smoothed to DC 350V to the lamp output. Then current resonance DC-DC converter which uses the DC 350V as an input converts the voltage and supplies S6V, +6V, +10V, +13V, +15.5V and –12V.

The boost-up-converter control IC, IC301, stabilizes AC rectified voltage to DC 350V. The current resonance DC-DC converter, IC303, turns FET Q102 and Q103 "ON/OFF" alternately using the drive transformer T103 and converts the voltage to secondary side through the converter transformer T101. At this time, the voltage of S6V at the secondary side is detected by IC402, the negative feedback to IC303 is carried out at photo coupler PH301 and then the voltage is stabilized. Other outputs are determined by the turn ratio of secondary side of T101, and the voltage rectified, smoothed, but not stabilized are stabilized through the series regulator. (+10V is stabilized at IC203, +13V at IC202, +15.5V at IC201.)

The voltage rectified and smoothed by D105 and C113 at primary winding of T101 is supplied as a $V_{CC}$ voltage of IC301, IC302 and IC303 on primary side ICs, and also the voltage rectified and smoothed by D106 and C114 is supplied as a gate bias voltage of D306 TRIAC (triode AC switch) which short-circuits the inrush current limiting resistor R305. Therefore, when the electric current resonance DC-DC converter stops to oscillate, the $V_{CC}$ voltage is not supplied so that the boost-up-converter stops to operate.

## 1-2. Output Control

When the output control 1 and 2 of connector A develops low, the voltage of approx. 14V is added to Q203 gate and pins 4 of IC203, IC201, and IC202 through R205 and R206 respectively, since the transistors Q201 and Q202 turn off. In this case, Q204, IC201, IC202 and IC203 turn off, the voltages of +6V, +10V, +15.5V and +13V are not developed.

When the output control 1 and 2 develop high, the transistors Q201 and Q202 turn on, so no voltage is added to the gate Q203, IC201, IC202 and IC203, described above, and the voltage of +6V, +10V, –15.5V and +13V are developed.

## 1-3. Voltage Switching

When the voltage switching terminal of connector C opens, pin 1 develops low, since the pin 2 of IC401 is 6V, higher than pin 2 (3V), the voltage adjusted to 16.3V is directly developed from IC201, since the status of Q205 turns off. When the voltage switching terminal develops ground potential, since pin 2 of IC401 develops 0V and the voltage of pin 2 develops low, pin 1 develops high, Q205 turns on, voltage-set-up resistor of R201 is short-circuited and the voltage of IC201 rises from 16.3V to 18.0V.

## 1-4. Over-voltage Protection

When the negative feedback circuit of current resonance DC-DC converter is shut down, the secondary side voltage control is unable to operate, the voltage begins to develop high without any restriction. At this time, when the voltage of S6V and +6V exceeds 8.5V, the base of transistor Q401 is biased through the zener diode D201, and turns on, and then the voltage higher than 7V is added to pin 6 (OVP) of IC303 through the photo coupler PH302. When the voltage higher than 7V is added to pin 6, IC303 is latched, all outputs are shut down. ( Boost-up-converter stops simultaneously, too.)

When the voltage is added to +10V, +13V, +15.5V lines from external side, (exceeding +15V for +10V line, 13V for +13 line and 20V for +15.5V line), on each line respectively through the zener diodes D202, D203 and D204, the base voltage of Q401 is biased passing, IC303 is latched in the same way as the above-mentioned, all outputs are shut down. When releasing the latch operation, stop to supply the commercial power supply and then re-supply the commercial power after more than approx. 120 seconds.

## 1-5. Over-current Protection

In S6V and +6V lines, the voltage drop owing to the current flowing in L203 is detected by pins 5 and 6 of IC401, when the total current amount exceeds 8A, pin 7 develops high and the voltage biasses the base voltage of transistor Q401 passing through the zener diode D402 and diode D401. In the same way as described in the item of the over-voltage protection, IC303 is latched and all outputs are shutdown. The method to release the latch operation is the same as the item of the over-voltage protection.

Over-current protection at +10V, +13V, +15.5V lines are carried out by the over-current protection characteristic provided with the series regulator ICs (IC203, IC202 and IC201). Refer to Fig. 1-5-1.

In this case, as only the line short-circuiting or overloading is protected, no effect appears on other outputs. The protection is released by removing the over current flowing condition.

When short-circuiting or overloading continues, the IC overheats and the overheat protection circuit inside the IC works to shut down the output voltage. In this case, the overheat protection is released by unloading the current and removing the overheat of IC.

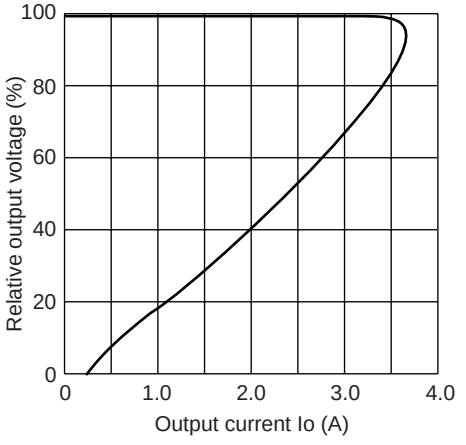



**Fig. 1-5-1**

**<Supplement>**

The over-current protection for lamp output detects the voltage drop of the current detection resistor R113 at between pins 9 and 10 of IC302. When voltage switching terminal of connector C opens (at 16.3V), the photo coupler PH303 turns off since pin 1 of IC401 develops low and the voltage of drop voltage at R113 is directly compared at pin 10 of IC302. When the lamp output current is from 0.7 to 0.9A, pin 8 develops high and the voltage higher than 7V is added to pin 6 of IC303. Then IC303 is latched and all outputs are shut down.

When the voltage switching terminal of connector C develops the ground potential (at 18.0V), pin 1 of IC401 develops high, PH303 turns on and the voltage of drop voltage at R113 and the voltage divided by R317 and R327 are compared at pin 10 of IC302. When the lamp output is from 1.05 to 1.35A, pin 8 of IC302 develops high, IC303 is latched and all outputs are shut down. The method to release the latch operation is the same as the over-voltage protection description.

## 1-6. Overheat Protection

As an overheat protection of the power supply, the temperature of switching FET Q301 of the boost-up-converter is detected. Positive characteristic thermistor TH301 for temperature detection is attached on the heat sink of Q301. When Q301 is overheated owing to the overload and/or defect of cooling fan, etc., the resistor value of TH301 increases abruptly, while the surface temperature exceeds approx. 120°C. Then the transistor Q302 turns on, the voltage higher than 7V is added to the pin 6 (OVP) of IC303, IC303 is latched and all outputs are shut down.

When releasing the latch operation, stop to supply the commercial power by canceling, cool enough after more than approx. 120 seconds, and then re-supply the commercial power.

# 2. LAMP POWER SUPPLY CIRCUIT (LAMP DRIVER)

## 2-1. Configuration

The lamp power supply cicrcuit receives a DC220 to 390V (primary side) from the system power supply and provides a AC voltage (70 to 100$V_{AC}$ at ever turning on the lamp) to turn on the lamp. Fig. 2-1-1 shows the block diagram.

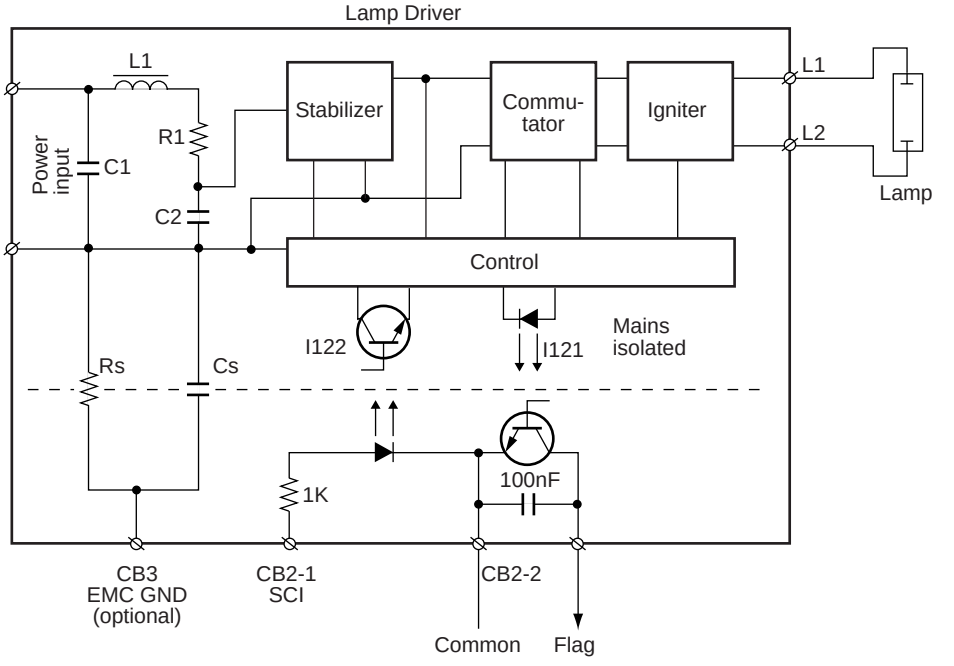



**Fig. 2-1-1**

The DC voltage is supplied to CB1 from the main power supply unit through an interlock switch. This voltage becomes AC input x 2$\sqrt{2}$ (= 340V for AC120V input) when the lamp is off. CB2 is a connector for the lamp on control signal input (SCI) and lamp off control signal output (FLAG). When +5V is applied to SCI (CB2-1) in the standby on, I122 FET transistor turns on, the igniter develops a high voltage pulse (5 to 25 kV), and the lamp starts to light up.

The pulse normally continues to be developed until the lamp turns on (for max. 3s.). But if the lamp does not turn on, I121 does not turn on, the voltage of CB2-3 develops high. I121 turns on and develops low after the lamp turned on, the igniter circuit stops the operation. Then the AC70 to 100V is applied to the lamp.

# 3. OPTICAL SYSTEM

## 3-1. Configuration

| | No. | Name | Description |
|---|---|---|---|
| Lamp unit | 1 | UHP lamp | Light source of the optical system. AC lighting system 120W, arc length 1.3 mm. As the arc length is shorter than the conventional metal halide lamp, the light source operates as an ideal light point source and this improves the light convergence factor. Also, the color temperature gets higher and this allows to reproduce more natural white color. |
| | 2 | Parabolic reflector | Parabolic reflector converges light emitted from the UHP lamp forward in approximate parallel light beams and illuminates the liquid crystal panel. |
| Mirror box unit | 3 | UV IR filter | Optical filter to pass necessary visible rays and cut unnecessary ultraviolet rays and infrared rays among light emitted from the UHP lamp. |
| | 4 | Multi-lenses A, B | Two multi-lenses A and B allow a circular beam light emitted from the light source to illuminate the square liquid crystal panel evenly, thus providing projected pictures with less brightness variation. |
| | 5 | Polarization light beam splitter (PBS) | Separates the illuminating light from the light source into P polarization light and S polarization light and leads both light to the multi-lens B with a little angle. |
| | 6 | Phase difference plate | Converts the polarization direction of incident light via the multi-lens B into another direction. Here, P polarization light waveform separated by PBS is converted into another S polarization light waveform. |
| | 7 | Condenser lens | Converges the illuminating light emitted from the light source into the liquid crystal panel. |
| | 8 | Dichroic mirror | Separates the white light emitted from the light source into RGB three primary colors. The white light emitted from the light source reflects B light using a dichroic mirror 1 and the RG lights pass through the dichroic mirror 1. Of the RG lights passed, G light is reflected by the dichroic mirror 2 and R light passes. |
| | 9 | Full reflection mirror | Reflection mirror to lead the R and B lights separated by the dichroic mirrors 1 and 2 to the liquid crystal panel. |
| | 10 | Field lens | Light transmitted through liquid crystal panel is converged in direction of focal point and effectively entered entrance pupil of the projection lens. |
| | 11 | Relay lens | In the R axis optical path which is longer than those of G, B, the relay lens works as a correction lens to arrange the illumination distribution of the liquid crystal panel surface with that of other liquid crystal panel. |
| | 12 | Incident side polarized plate/Phase difference plate | The illumination lights separated into RGB have the S polarizing waveform component in processing the PBS and phase difference plate operation previously described.<br>The incident side polarized plate arranges the illumination light more effective direct polarizing waveform. The phase difference plate used works to converge the S polarizing waveform into the P polarizing waveform which fits to the transparent axis of the liquid crystal panel.<br>Since the phase difference plate possesses the wavelength characteristics for light, each RGB axis employs exclusive phase difference plate. These polarizing plates and difference plates are constructed in one plate by attaching each other, and put on a glass plate.<br>To increase the color purity ratio of three primary colors, the glass plate possess the dichroic filter characteristics for RG axis. |
| Prism unit | 13 | Liquid crystal panel | Light exit side polarized plate is put on the light exit plane. When no signal voltage is applied, the polarization direction of transmission light rotates by 90 degrees. When a voltage is applied, the polarization direction is controlled owing to the voltage applied. That is, the liquid crystal panel employs such general TN type liquid crystal. In this model, the incidence/exit polarization plate is placed (in normally white mode) so that the light transmission amount becomes maximum (white) when no voltage is added and the light transmission amount becomes minimum (black) when maximum voltage is added.<br>According to the liquid crystal panel specification, exclusive panel for each RGB axis is employed and shown by identification seals. |
| | 14 | Cross prism | Works to mix RGB lights passed through the liquid crystal panel. |
| Projection lens | 15 | Projection lens | Demodulated by the video signal on the liquid crystal panel and projects pictures displayed on the liquid crystal at a screen. Light axis of the projection lens is set at upper side of center of the liquid crystal panel and this realizes easy viewing of the panel because the projected screen position is upper than the unit position. The projected light shows S polarizing waveform and is compatible with the polarizing screen.<br>The projection lens employs the zoom & focus system and allows to project enlarging a picture upto maximum approx. 300 inch. |

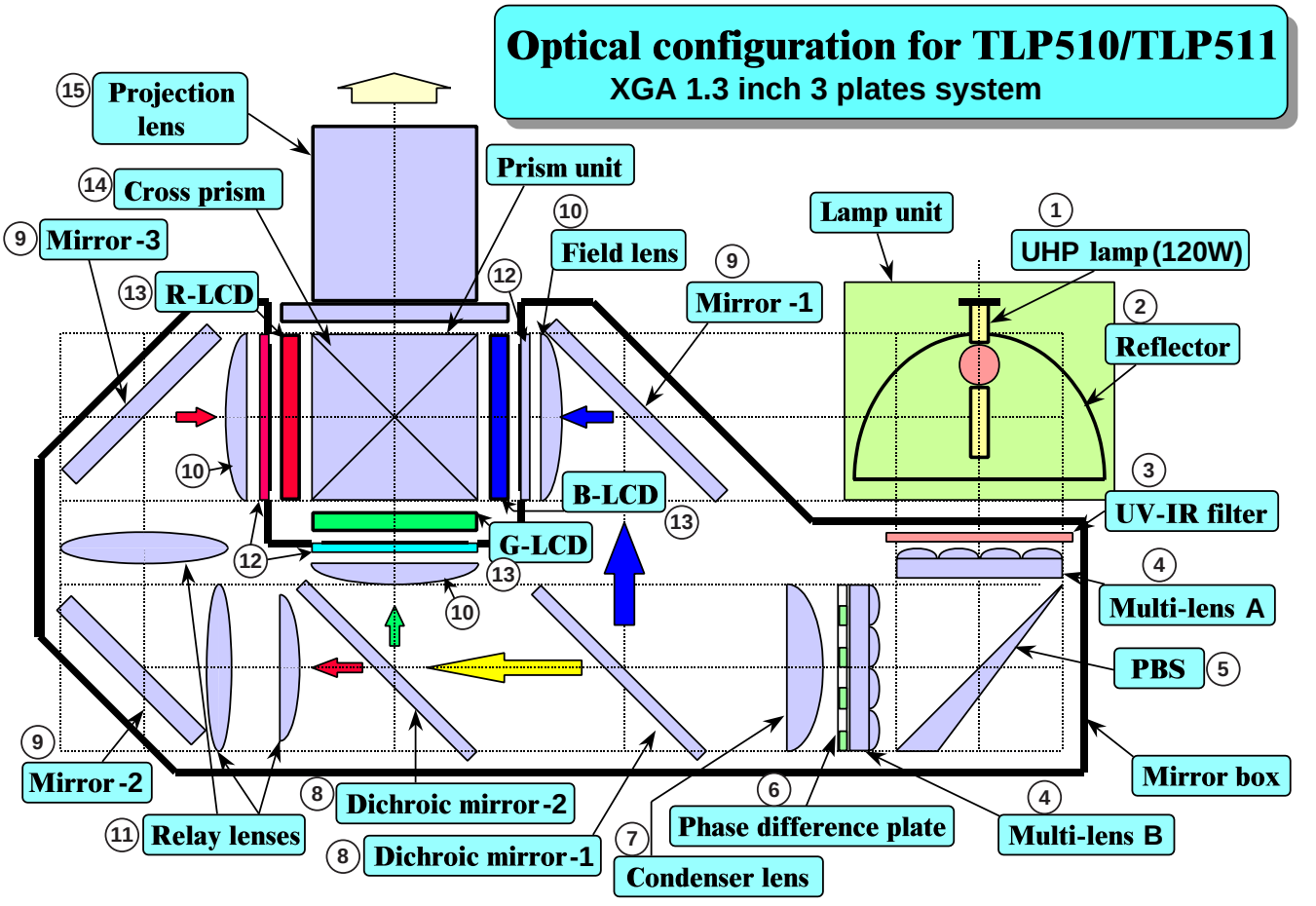



**Fig. 3-1-1 Optical configuration diagram**

# 4. R.G.B. DRIVE CIRCUIT

## 4-1. Outline

The outline of RGB drive circuit is described below using the G process of the RGB drive circuit as an example.

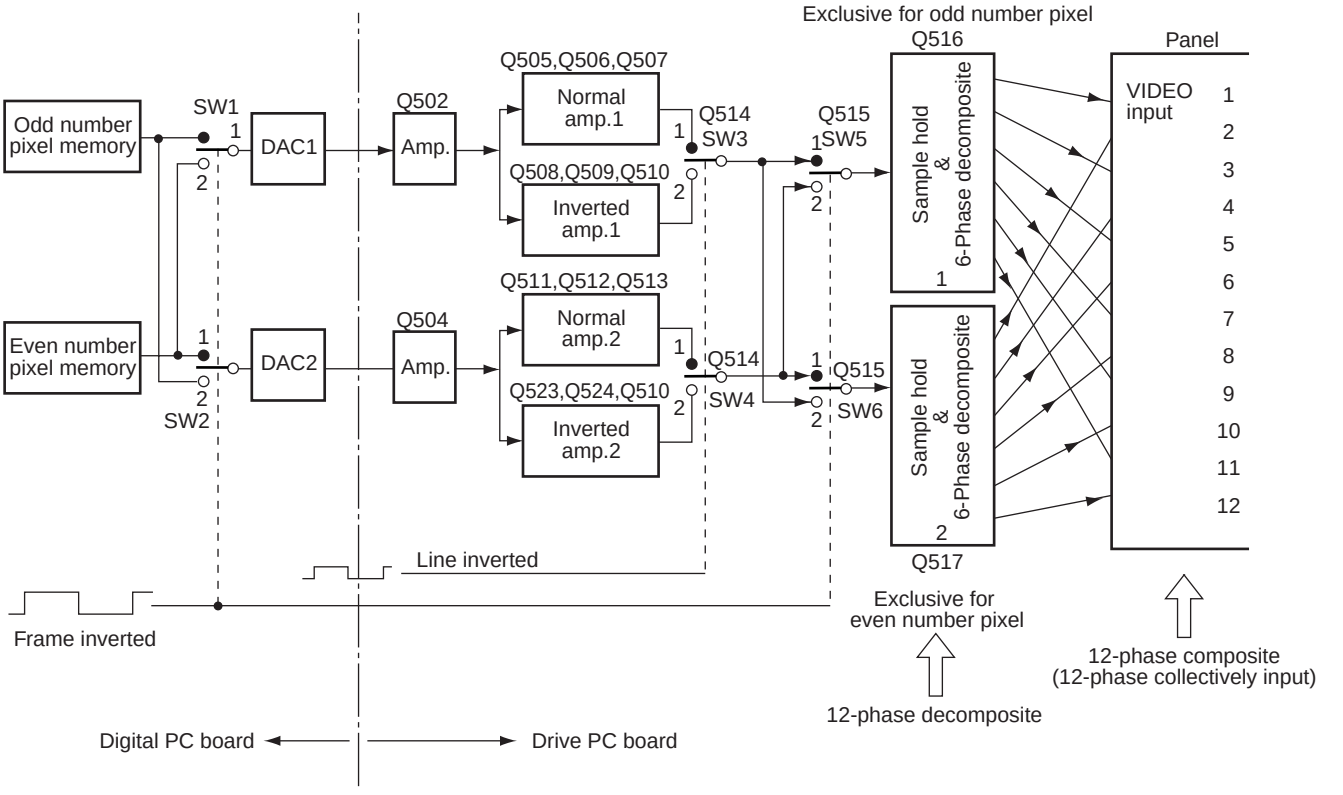



**Fig. 4-1-1**

In the panel, 1024 pixels are arranged in a horizontal direction and 768 lines of the pixels are in a vertical as shown in Fig. 4-1-2.

As an H inverted drive system is employed, the panel input signal waveform is as shown in Fig. 4-1-3.

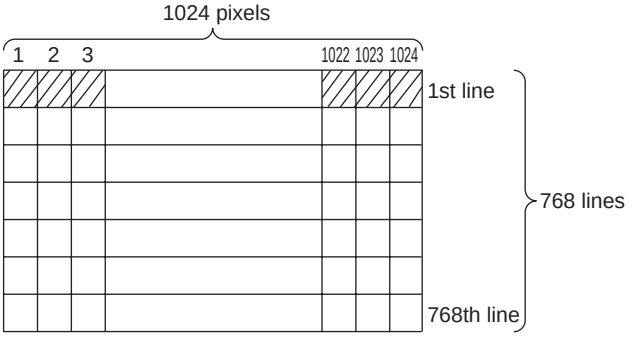



**Fig. 4-1-2**

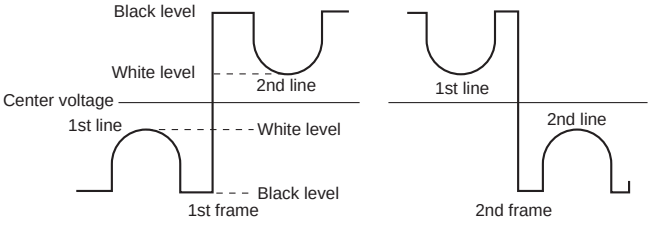



**Fig. 4-1-3**

The signal as shown in Fig. 4-1-1 is separated into the odd and even pixels at the digital PC board. After the signal process is carried out in the drive PC board, the odd and even pixel signals are synthesized to decomposite the signal on the panel.

Referring to Fig. 4-1-1, the operation principle is described.

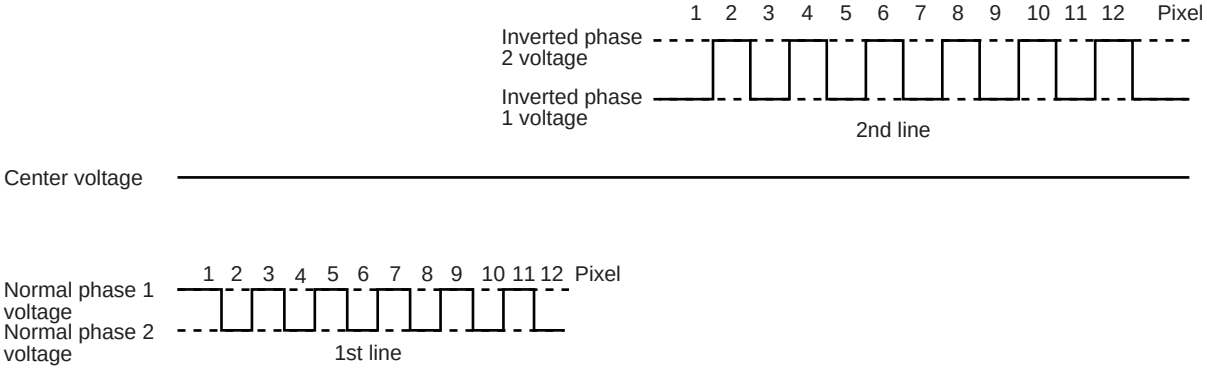
When assuming;

1) the signal passing through DAC1 ® Q502 ® Normal amp. 1 ® SW31 ® SW5 ® Q516 to the positive phase 1,
2) the signal passing through DAC1 ® Q502 ® inverted amp. 1 ® SW32 ® SW5 ® Q516 to the inverted phase 1,
3) the signal passing through DAC2 ® Q504 ® Normal amp. 1 ® SW41 ® SW6 ® Q517 to the positive phase 2 and
4) the signal passing through DAC2 ® Q504 ® inverted amp. 2 ® SW42 ® SW6 ® Q517 to inverted phase 2,

the AC and DC levels of the positive phases 1, 2 and the inverted phases 1, 2 are expected to be the same.

However, each voltage will vary slightly owing to the adjustment variation. In this case, each frame signal is assumed as follows.

**<1st frame>**


1 2 3 4 5 6 7 8 9 10 11 12 Pixel
Inverted phase 2 voltage
Inverted phase 1 voltage
2nd line
Center voltage
1 2 3 4 5 6 7 8 9 10 11 12 Pixel
Normal phase 1 voltage
Normal phase 2 voltage
1st line

**<2nd line>**

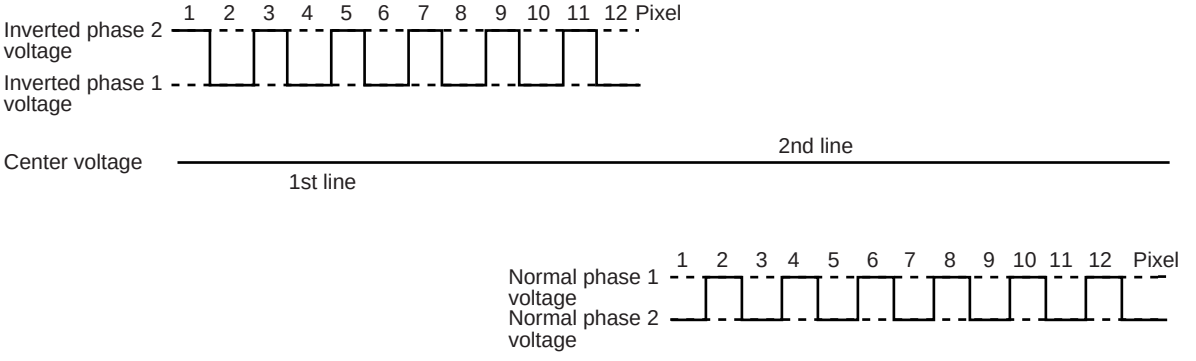

1 2 3 4 5 6 7 8 9 10 11 12 Pixel
Inverted phase 2 voltage
Inverted phase 1 voltage
Center voltage
2nd line
1st line
1 2 3 4 5 6 7 8 9 10 11 12 Pixel
Normal phase 1 voltage
Normal phase 2 voltage

**Fig. 4-1-4**

As shown in Fig. 4-1-4, even if a slight level difference occurs among the positive phases 1, 2 and inverted phases 1, 2 signals (approx. 100 mV), the level difference will be decreased visually by reducing the level variation of the same line between each frame and inverting the pixel voltage of the adjacent lines (1st line and 2nd line) between each frame.

## 4-2. Operation Description

The video signal of the odd number pixel (even number pixel) is sent to Q501 (Q503) base and supplied to pin 16 of Q502 (Q504), LM1201M. The signal is clamped at pin 16 and the pedestal voltage is adjusted at pin 6 after the DC level is stabilized and then AC level is adjusted at pin 3.

The signal is developed from pin 8, supplied to the buffer circuits of Q505 – Q507 and Q511 – Q513, and supplied to the inverted circuits of Q508, Q509, Q510, Q523, Q525 and Q510. These signals are supplied to pins 5, 6, 8, 13, 15 and 16 of 12 phases development IC. CXA2504N, Q516 and Q517 of sample-and-hold passing through the SW circuit composed of Q514 and Q515. The signals are developed from pins 37, 35, 33, 25 and 23 for each input.

The signals at pins 4, 7, 14 are used as bias input and the bias inputs set the center DC voltage of output equal to the bias voltage.

Q519 works to suppress the noise occurred at 12 phases collective input process of the panel.

### 4-2-1. Outline of Liquid Crystal Panel

The liquid crystal panel module is an active matrix panel with a built-in driver of multi-crystal silicon. The liquid crystal panel module is designed for use of color projectors in combination with an enlargement projection system and dichroic mirror.

**<Basic specification>**

(1) Screen size 26.624 (W) x 19.968 (H)

(2) Pixel number 1024 (W) x 768 (H)

(3) Applicable to XGA

(4) Monochrome panel

(5) Drive system H inverted drive

(6) Dot clock 65 MHz

(7) Inverted function for UP/DOWN/LEFT/RIGHT directions

### 4-2-2. Basic Component

**Table 4-2-1 Terminal description**

| Pin No. | Name | Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---|---|---|---|---|---|---|---|
| 1 | DT | 10 | VID7 | 19 | $\overline{\text{DIRX}}$ | 28 | VID10 |
| 2 | $\overline{\text{CLY}}$ | 11 | VID5 | 20 | DIRX | 29 | VID12 |
| 3 | CLY | 12 | VID3 | 21 | ENB2 | 30 | LCCOM |
| 4 | VDDY | 13 | VID1 | 22 | ENB1 | 31 | N.C. |
| 5 | NRS2 | 14 | VSSX | 23 | VSSX | 32 | NRG |
| 6 | NRS1 | 15 | $\overline{\text{CLX}}$ | 24 | VID2 | 33 | DY |
| 7 | LCCOM | 16 | CLX | 25 | VID4 | 34 | DIRY |
| 8 | VID11 | 17 | DX | 26 | VID6 | 35 | $\overline{\text{DIRY}}$ |
| 9 | VID9 | 18 | VDDX | 27 | VID8 | 36 | VSSY |

**Table 4-2-2 Input terminal function description**

| Name | Function |
|---|---|
| DX | Start pulse input terminal of X shift register composing X driver. |
| CLX, $\overline{\text{CLX}}$ | Transfer clock input terminal X shift register composing X driver |
| DIRX, $\overline{\text{DIRX}}$ | X driver driving direction switch input terminal (DIRX = H R shift, DIRX = L L shift) |
| ENB1 – ENB2 | X driver enable pulse input terminal |
| VID1 – VID12 | X driver video signal input terminal |
| DY | Start pulse input terminal of Y shift register composing Y driver. |
| CLY, $\overline{\text{CLY}}$ | Transfer clock input terminal of Y shift register composing Y driver. |
| DIRY, $\overline{\text{DIRY}}$ | Transfer clock input terminal of Y shift register composing Y driver. (DIRX = H Down shift, DIRX = L Up shift) |
| LCCOM | Diagonal electrode potential input terminal of liquid crystal panel |
| VDDX | X driver positive power supply input terminal |
| VDDY | Y driver positive power supply input terminal |
| VSSX | X driver negative power supply input terminal |
| VSSY | Y driver negative power supply input terminal |
| NRG | Drive signal input terminal for auxiliary signal circuit |
| NRS1 – NRS2 | Auxiliary signal input terminal |

# 5. MICROPROCESSOR

## 5-1. System Outline

The system microprocessor has features as shown below.

In considering easy maintenance for specification modification, etc., the program content is written in the built-in non-volatile memory.

The program is also developed in considering use of structured notation, parts modularity, and multi filling system.

Major functions of the system microprocessor are as follows.

### 5-1-1. System Control

- Microprocessor program write process
- Non-volatile memory control process
- Remote control reception process
- RS-232C transmission/reception process
- Status read process
- On-screen display process

### 5-1-2. Normal Control

| | |
|---|---|
| • Power | ON/OFF (Main/Fan/Lamp) |
| • Input switch | (RGB/Video/Camera) |
| • Sound volume control | UP/DOWN |
| • Menu | |
| • Adjust | (Up/Down/Left/Right) |
| • All mute | ON/OFF |
| • Audio mute | ON/OFF |
| • Display | ON/OFF |
| • Freeze | ON/OFF |
| • Resize | ON/OFF |
| • Focus | UP/DOWN (at camera use) |
| • Zoom | UP/DOWN (at camera use) |

### 5-1-3. Adjustment Control

- Video controls (high & low brightness ratio, brightness, color density, tint, sharpness)
- Panel adjustments (V position, H position, phase, clock, user registration, user read-out)
- Mode adjustments (Wide, MIC, OSD mute, projection)
- Language adjustments (English, Japanese, French, German, Spanish, Italian)

### 5-1-4. Adjustment Control at Factory Delivery

- Video sub adjustments (RGB gain, sub-bright)
- Drive adjustments (each item for panel controls, RGB trimming)

Fig. 5-1-1 shows the system block diagram.

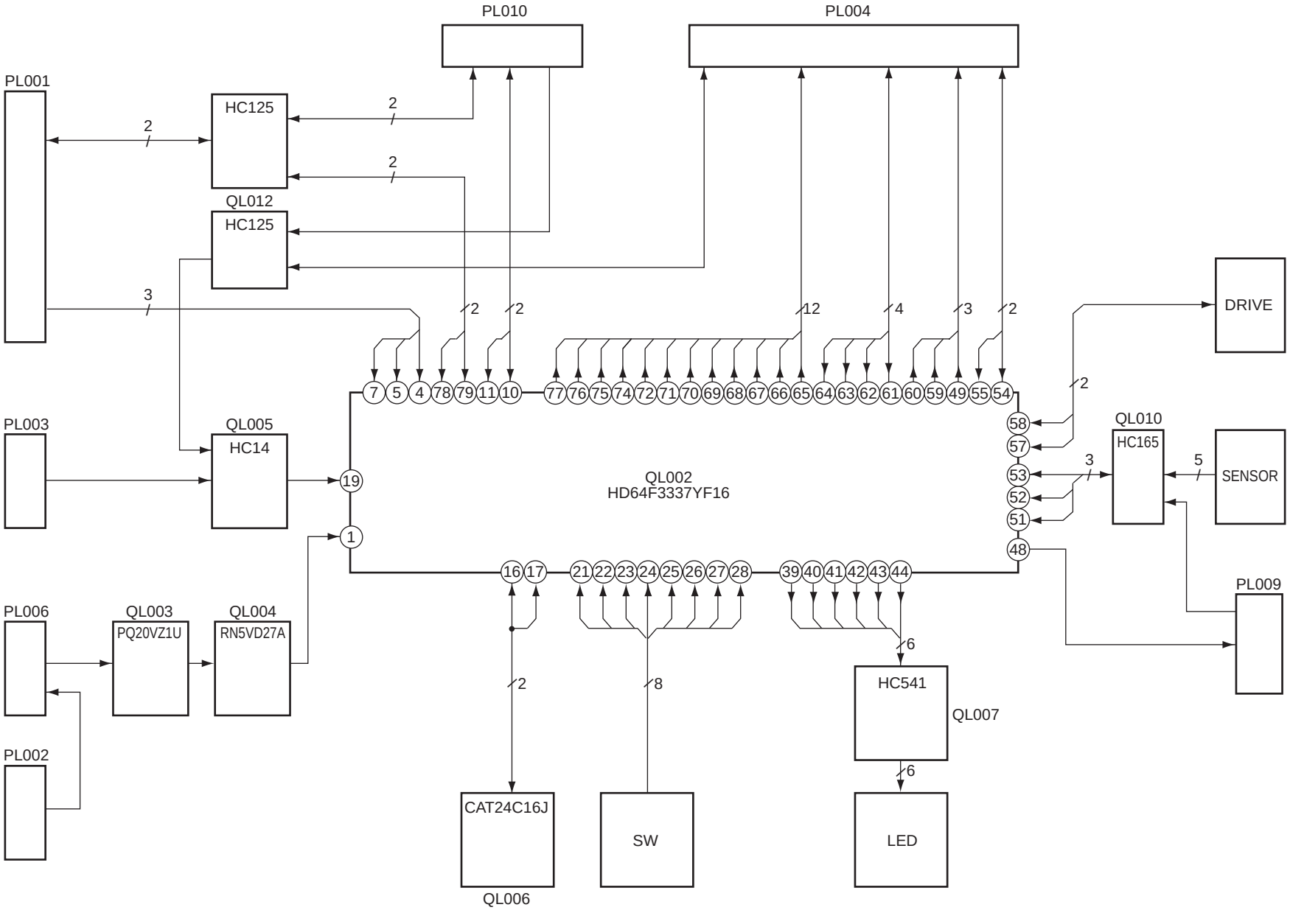



**Fig. 5-1-1 System block diagram**

## 5-2. System Microprocessor

The system microprocessor QL002 employs an 8 bit micro-controller (HD64F3337YF16).

In this system microprocessor, a program area is provided inside the non-volatile memory.

Using an exclusive data-writer allows easy maintenance of the system microprocessor when specification modification, bug correction, etc. will occur.

Table 5-2-1 shows the terminal functions of the system microprocessor.

**Table 5-2-1 Terminal functions of the system microprocessor**

| Pin No. | Name | Function | I/O | Pin No. | Name | Function | I/O |
|---|---|---|---|---|---|---|---|
| 1 | RES | Reset input | I | 41 | LED2 | LED data 2 | O |
| 2 | XTAL | Clock input for oscillation | I | 42 | LED3 | LED data 3 | O |
| 3 | EXTAL | Clock output for oscillation | O | 43 | LED4 | LED data 4 | O |
| 4 | MD1 | Mode 1 | I | 44 | LED5 | LED data 5 | O |
| 5 | MD0 | Mode 2 | I | 45 | MAIN. PW | Main power supply swtich | O |
| 6 | NMI | Priority interruption | I | 46 | FAN. PW | Fan power supply switch | O |
| 7 | FVPF | Memory write voltage | I | 47 | $V_{CC2}$ | Digital power supply | I |
| 8 | VCC1 | Digital power supply | I | 48 | LAMP. PW | Lamp power supply switch | O |
| 9 | WDT | Not used | O | 49 | OSDL | OSD load | O |
| 10 | RXD0 | RS-232C reception for camera | I | 50 | DDCV | Not used | I |
| 11 | TXD0 | RS-232C transfer for camera | O | 51 | SENL | Sensor load | O |
| 12 | GND1 | Digital ground | I | 52 | SENC | Used for sensor | O |
| 13 | SDA | Not used | I/O | 53 | SEND | Used for sensor | I |
| 14 | f | Oscillation clock | O | 54 | VD0C | Video $I^2C$ clock | O |
| 15 | SEL | Remote controller selection | O | 55 | VD0D | Video $I^2C$ data | I/O |
| 16 | EEPCK | Non-volatile memory clock | O | 56 | GND2 | Digital ground | I |
| 17 | EEPDT | Non-volatile memory data | I/O | 57 | DRVC | Drive $I^2C$ clock | O |
| 18 | VD | Not used | I | 58 | DRVD | Drive $I^2C$ data | O |
| 19 | REMOCON | Remote controller reception | I | 59 | OSDC | OSD clock | O |
| 20 | AUX | Not used | O | 60 | OSDD | OSD data | O |
| 21 | KEY0 | Key input 0 | I | 61 | PLLU | PLL enable | O |
| 22 | KEY1 | Key input 1 | I | 62 | SYGL | SYG load | O |
| 23 | KEY2 | Key input 2 | I | 63 | SYGC | SYG clock | O |
| 24 | KEY3 | Key input 3 | I | 64 | SYGD | SYG data | I/O |
| 25 | KEY4 | Key input 4 | I | 65 | D0 | T-FORC data 0 | O |
| 26 | KEY5 | Key input 5 | I | 66 | D1 | T-FORC data 1 | O |
| 27 | KEY6 | Key input 6 | I | 67 | D2 | T-FORC data 2 | O |
| 28 | KEY7 | Key input 7 | I | 68 | D3 | T-FORC data 3 | O |
| 29 | AVCC | Analog power supply | I | 69 | D4 | T-FORC data 4 | O |
| 30 | AD0 | Not used | I | 70 | D5 | T-FORC data 5 | O |
| 31 | AD1 | Not used | I | 71 | D6 | T-FORC data 6 | O |
| 32 | AD2 | Not used | I | 72 | D7 | T-FORC data 7 | O |
| 33 | AD3 | Not used | I | 73 | GND3 | Digital ground | I |
| 34 | AD4 | Not used | I | 74 | CLK | T-FORC clock | O |
| 35 | AD5 | Not used | I | 75 | R/W | T-FORC read/write | O |
| 36 | AD6 | Not used | I | 76 | ENB | T-FORC enable | O |
| 37 | AD7 | Not used | I | 77 | RST | T-FORC reset | O |
| 38 | AGND | Analog ground | I | 78 | TXD1 | RS-232C transfer for control | O |
| 39 | LED0 | LED data 0 | O | 79 | RXD1 | RS-232C reception for control | I |
| 40 | LED1 | LED data 1 | O | 80 | SCL | Not used | O |

## 5-3. Power Supply Reset Process

In the power supply reset process, power supply reset IC (RN5VD27A), QL004 is employed.

The reset IC,QL004, develops the reset signal when the power supply voltage for the microprocessor varies and becomes lower than the specified voltage, and sends the signal to the reset terminal of the system microprocessor (QL002).

## 5-4. Non-volatile Memory Control Process

In the non-volatile memory process, data reading and saving for various adjustments are carried out on the non-volatile memory, QL006 (CAT24C16J).

When the power (AC) is on, all the adjustment data are read out by the system microprocessor (QL002), then the previous status is realized.

When saving the data, all the adjustment data are written by the system microprocessor (QL002), then the current status is preserved.

However, if a failure (such as power interruption due to lightning, etc.) occurs during the adjustment data writing, a data error may occur. If the data is determined as incorrect, the initial data memorized on the system microprocessor (QL002) is read out and stored on the non-volatile memory.

## 5-5. Remote Control Reception Process

In the remote control reception process, a remote control unit (CT-9925) connected to the remote control terminal emits a remote control signal and a remote control signal receive section on the front panel, the rear panel or the camera arm (for TLP511) decodes the signal.

The remote control signals for rear panel and camera section (for TLP511) are selected by QL012 buffer (TC74HC125AF). Then both signals are mixed with the remote control signal for front panel through QL005 buffer (74HC14AF).

Finally, the signal mixed is supplied to the remote control terminal of the system microprocessor (QL002).

## 5-6. RS-232C Transmission/Reception Process

In the RS-232C transmission/reception process, an RS-232C signal entered through the RS-232C connector (D-SUB 9P) is decoded in the RS-232C interface (mPD4721), and fed to RXD1 terminal of the system microprocessor (QL002).

In the RS-232C transmission process, RS-232C signal developed from TXD0 terminal of the system microprocessor (QL002) is decoded in the RS-232C interface (mPD4721) and fed to the camera microprocessor section.

## 5-7. Status Read Process

In the status read process, the following status shown in the table below are read by QL010 (74HC165AF) and the error process corresponding to each status is carried out.

Table 5-7-1 shows the contents of the status read signals and the logic.

**Table 5-7-1 The contents of the status read signals and the logic**

| **Signal name** | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| **Pin No.** | 11 | 12 | 13 | 14 | 3 | 4 | 5 | 6 |
| **QL010** | FAN1. ER | FAN1. SW | FAN2. ER | | TEMP1. ER | | LAMP. ER | MAIN. ER |
| **(L)** | Abnormal | Normal | Abnormal | | Normal | | Abnormal | Abnormal |
| **(H)** | Normal | Abnormal | Normal | | Abnormal | | Normal | Normal |

## 5-8. Status Display Process

In the status display process, two-color lighting LEDs of DL037, DL038 and DL039 turn ON for each kind of status shown in the table below by using LED0 to LED5 terminal output of the microprocessor.

## 5-9. On-screen Display Process

In the on-screen display process, control signals are supplied to the OSD display IC QX003 (CD0016AM), and the OSD display IC generates character display signals at the timing determined by VD, HD and clock supplied to the IC separately.

**Table 5-8-1 Contents of the status display signals and the logic**

| ON | LAMP | TEMP | Function | Status | Countermeasure |
|---|---|---|---|---|---|
| X | X | X | Stand-by power supply abnormality | At AC cord plugged | Repair |
| Green | Green | Green | Non-volatile memory OK | At AC cord plugged | Normal |
| Red | Red | Red | Non-volatile memory NG | At AC cord plugged | At initial time |
| Orange | X | X | Stand-by | At power off | Normal |
| Green | X | X | Lamp ON | At power on | Normal |
| Green | (Green) | X | Lamp Heat-up | At power on | Normal |
| Green | Green | X | Lamp Lighting | During power on | Normal |
| Green | X | X | Lamp OFF | At power off | Normal |
| Orange | (Green) | X | Lamp cool-down | At power off | Normal |
| Red | X | X | Main power supply abnormality | At power On/During | Repair |
| Red | Red | X | Lamp no-lighting | At power On/During | Repair or preparation failure |
| Red | Orange | X | Lamp lighting-lifetime | At power on | Operates after approx. 2500 H operation |
| Red | X | (Red) | Suction fan stop | At power on | Repair |
| Red | X | (Orange) | Exhaust fan stop | At power on | Repair |
| Red | X | (Green) | Fan filter open | Ever | Close |
| Red | X | Red | Temperature sensor abnormality | Ever | Lower internal temperature of the unit. |

X: Lighting OFF

( ): Blinking

## 5-10. Video System Control Process

In the video system control process, control signals are supplied to various video system process ICs shown in the table below. Table 5-10-1 shows the $I^2C$ control for each kind of video system.

## 5-11. Panel System Control Process

The panel system control process supplies various control signals to the panel system control ICs shown in the table below.

Table 5-11-1 shows the IC control for each kind of panel system.

**Table 5-10-1 $I^2C$ control for each kind of video system**

| Part No. | Type name | Process |
|---|---|---|
| QV001 | CXA1855Q<br>(Custom: $90) | I/O SW process |
| QV002 | TC9090N<br>(Custom: $B2) | Color signal process (3D Y/C separation) |
| QV005 | TDA9141<br>(Custom: $8A) | Sync detection process (Custom: $8B)<br>Signal kinds identification (NTSC/PAL/SECAM, etc.) |
| QV008 | TDA4780<br>(Custom: $88) | Video control (Density, hue) |
| QV007 | TDA4672<br>(Custom: $88) | Video control (Sharpness control) |
| QV045 | CXA1315M<br>(Custom: $40) | Input SW, MIC SW<br>Volume, mute, MIC gain |
| QB025 | CXA1315M<br>(Custom: $44) | Brightness, contrast, RGB gain<br>Sync information |
| QV057 | M62320FP<br>(Custom: $71) | Camera ON/OFF (for TLP511), focus, zoom reading<br>Fan switch open |

**Table 5-11-1 IC control for each kind of panel system**

| Part No. | Type name | Process |
|---|---|---|
| QX004 | SYG<br>(TC160G54AF1137) | Various kinds of screen display process (position, picture frame, property)<br>Screen position control (Vertical position, horizontal position) |
| QX007 | CXA3106 | Screen position control (sampling phase, sampling frequency) |
| QX204<br>QX404<br>QX604 | TFORC<br>(TC203E2651AF-01) | Picture frame control (R)<br>Picture frame control (G)<br>Picture frame control (B) |
| QX001 | M62320FP<br>(Custom: $78) | Panel mode control<br>A/D sample phase (R) |
| QX002 | M62320FP<br>(Custom: $7A) | A/D sample phase (G)<br>A/D sample phase (B) |

## 5-12. Drive System Control Process

In the drive system control process, the control signal is supplied to each kind of drive system process ICs shown in the the table below.

Table 5-12-1 shows each kind of the drive system IC control.

**Table 5-12-1 Each kind of the drive system IC control**

| Part No. | Type name | Process |
|---|---|---|
| Q701 | M62399FP (Custom: $90) | Process relative to R drive |
| Q702 | M62399FP (Custom: $92) | Process relative to G drive |
| Q703 | M62399FP (Custom: $94) | Process relative to B drive |
| Q704 | M62399FP (Custom: $96) | Process relative to VCOM, NR |
| Q705 | M62399FP (Custom: $98) | Process relative to NR, Bias |

## 5-13. Various Display Modes

In this system, various LED display patterns are provided in relation to the display modes shown in Table 5-8-1. Operation processes from the status of AC cord plugged to that of power on and power off will be given below.

(1) Data of the non-volatile memory are checked when the AC cord is plugged, and all the LED are turned on in red in the initial use. In second or later use, all the LEDs are turned on in green and the unit enters the standby status.

(2) In the standby status, only the ON/STANDBY LED is turned on in orange, and the main power is off and the lamp power is also off.

(3) When the power is on by pressing the ON/STANDBY key, the unit enters a normal status in passing through following processes.

1) The main power is on, and ON/STANDBY LED turns on in green.
2) The fan power is on, and the fan starts to rotate.
3) The lamp power is on, and LAMP LED blinks in green for about 3s.
4) With the lamp turned on, LAMP LED turns on in green and the unit enters the normal status.

(4) If the lamp does not turn on, ON/STANDBY LED turns on in orange, and the LAMP LED blinks in green for about 1 min. and then the unit returns to the standby status.

(5) In the normal status, ON/STANDBY LED and the LAMP LED are turned on in green, and the main power and the lamp power are turned on.

(6) When the power is turned off by pressing the ON/STANDBY key, the unit enters the standby status in passing through following processes.

1) When the lamp power is turned off, ON/STANDBY LED turns on in orange.
2) The LAMP LED blinks in green for about 1 min. For this period the lamp can not be turned on again by the ON/STANDBY key.
3) When blinking of the LAMP LED stops, only the ON/STANDBY LED turns on in orange. After this, the lamp can be turned on again by the ON/STANDBY key.

(7) Moreover, the fan works for about 2 min. to lower temperature of the unit. When the main power turns off, the fan also stops and returns to the standby status.

(8) If an error occurs due to some causes, the ON/STANDBY LED turns on in red, and the error information is kept in the display status of the LAMP and TEMP LEDs. When the error is detected, the unit enters the standby status after cooling down process for about 2 min. In this case, if the error status continues, the error display is also kept and any key entry is not accepted.

## 5-14. Applicable Signal

Various kinds of signals are used as the applicable signals in the preset mode (standard value) as shown in Table 5-14-1. For the signals not fit to the preset modes, a user mode is provided.

In the preset modes, the applicable signals are based on the VESA standard, so the sample frequency (CLOCK adjustment in the panel menu) is not used, but the adjustment is allowed only in the user mode.

In other mode, the signal line number is detected to allow the separate adjustment in the VGA system (basically effective for line number of 480 lines), SVGA system (basically effective for line number of 600 lines) and XGA system (basically effective for line number of 768 lines).

In the user mode of SGA system (900 line system and 1024 line system), the input signal is applicable to the plain display mode. That is, the signal is displayed in different two ways owing to the line number in vertical direction.

**Table 5-14-1 Applicable signal**

| Signal | | Resolution | | Frequency | | | All | | Sync | Operation | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode | Content | H | V | H (kHz) | V (Hz) | Clock (MHz) | H | V | H/V | Corre-spondence | Remarks |
| NTSC | NTSC | 664 | 484 | 15.734 | 59.940 | 12.590 | 800 | 525 | N/N | O | Video input |
| PAL | PAL | 756 | 574 | 15.625 | 50.000 | 12.500 | 800 | 625 | N/N | O | Video input |
| V60 | VGA 60 Hz | 640 | 480 | 31.470 | 59.940 | 25.175 | 800 | 525 | N/N | O | |
| V72 | VGA 72 Hz | 640 | 480 | 37.861 | 72.809 | 31,500 | 832 | 520 | N/N | O | |
| V75 | VGA 75 Hz | 640 | 480 | 37.500 | 75.000 | 31.500 | 840 | 500 | N/N | O | |
| V85 | VGA 85 Hz | 640 | 480 | 43.269 | 85.008 | 36.000 | 832 | 509 | N/N | O | |
| M13 | MAC-13” | 640 | 480 | 35.000 | 66.667 | 30.240 | 864 | 525 | N/N | O | |
| 24K | PC98-STD | 640 | 400 | 24.830 | 56.420 | 21.053 | 848 | 444 | N/N | O | |
| T70 | VGA 70 Hz | 720 | 350 | 31.470 | 70.020 | 28.322 | 900 | 450 | P/N | D | |
| T70 | VGA 70 Hz | 720 | 400 | 31.470 | 70.020 | 28.322 | 900 | 450 | N/P | D | |
| T70 | VGA 70 Hz | 640 | 350 | 31.470 | 70.020 | 28.322 | 800 | 450 | P/N | O | |
| T70 | VGA 70 Hz | 640 | 400 | 31.470 | 70.020 | 28.322 | 800 | 450 | N/P | O | |
| T85 | VGA 85 Hz | 640 | 350 | 37.861 | 85.080 | 31.500 | 832 | 445 | P/N | O | |
| T85 | VGA 85 Hz | 640 | 400 | 37.861 | 85.080 | 31.500 | 832 | 445 | N/P | O | |
| T85 | VGA 85 Hz | 720 | 400 | 37.927 | 85.039 | 35.500 | 936 | 446 | N/P | D | |
| S56 | SVGA 56 Hz | 800 | 600 | 35.156 | 56.250 | 36.000 | 1024 | 625 | N/N | O | |
| S60 | SVGA 60 Hz | 800 | 600 | 37.879 | 60.317 | 40.000 | 1056 | 628 | N/N | O | |
| S72 | SVGA 72 Hz | 800 | 600 | 48.077 | 72.188 | 50.000 | 1040 | 666 | N/N | O | |
| S75 | SVGA 75 Hz | 800 | 600 | 46.875 | 75.000 | 49.500 | 1056 | 625 | N/N | O | |
| S85 | SVGA 85 Hz | 800 | 600 | 53.674 | 85.061 | 56.250 | 1048 | 631 | N/N | O | |
| M16 | MAC-16” | 832 | 624 | 49.724 | 74.550 | 57.283 | 1152 | 667 | N/N | O | |
| X60 | XGA 60 Hz | 1024 | 768 | 48.363 | 60.004 | 65.000 | 1344 | 806 | N/N | O | |
| X70 | XGA 70 Hz | 1024 | 768 | 56.476 | 70.069 | 75.000 | 1328 | 806 | N/N | O | |
| X75 | XGA 75 Hz | 1024 | 768 | 60.023 | 75.029 | 78.750 | 1312 | 800 | N/N | O | |
| X85 | XGA 85 Hz | 1024 | 768 | 68.677 | 84.997 | 94.500 | 1376 | 808 | N/N | O | |
| M21 | MAC-21” | 1152 | 870 | 100.000 | 68.653 | 75.030 | 1456 | 915 | N/N | X | Plain display |
| SXGA1 | 1152 system | 1152 | 864 | 108.000 | 67.500 | 75.000 | 1600 | 900 | N/N | X | Plain display |
| SXGA2 | 1280 system | 1280 | 1024 | 135.000 | 79.976 | 75.025 | 1688 | 1066 | N/N | X | Plain display |

- In the sync column of Table 3-14-1, P shows the positive polarity and N shows the negative polarity.
- In the operation column, O shows a standard mode, D shows pull-in mode, X shows plain display mode.

## 5-15. RS-232C Control Method

Signals are connected to the RS-232C connector in a straight format as shown in Table 5-15-1 RS-232C connection signals. This is because a crossing connection is provided inside the unit. Communication conditions are set to meet the conditions given in Table 5-15-2.

Table 5-15-3 shows the command list of RS-232C.

When transmitting the command, be always sure to keep 100 ms interval between each command. Moreover, the process time is required for a while when turning the power ON/OFF and/or selecting the input mode. So in such cases, also be always sure to keep enough intervals between the commands.

**Table 5-15-1 RS-232C connection signals**

| Pin No. | Signal name | Signal content | I/O |
|---|---|---|---|
| 2 | RXD | Receive data | I |
| 3 | TXD | Transmit data | O |
| 4 | DTR | Data terminal ready | O |
| 5 | S. G | Signal ground | I |
| 6 | DSR | Data set ready | I |
| 7 | RTS | Transmission request | O |
| 8 | CTS | Transmission enable | I |

**Table 5-15-2 RS-232C communication conditions**

| Item | Conditions |
|---|---|
| Communication system | Transmission speed 9600 baud, No parity, Data length 8 bit, Stop bit: 1 bit |
| Communication type | STX (1 byte) + CMD (3 byte) + ETX (1 byte) = 1 block<br>STX is 02h, ETX is 03h, CMD is command string (Uppercase character) |

**Table 5-15-3 RS-232C command list**

| Item | Command | Content | Item | Command | Content |
|---|---|---|---|---|---|
| Normal status | PON | Power supply ON | Panel | PVP | Vertical position |
| | POF | Power supply OFF | | PHP | Horizontal position |
| | IN1 | Video input | | PPH | Sampling phase |
| | IN2 | RGB input | | PCK | Sampling frequency |
| | IN3 | Camera input | | PL0 | |
| | VUP | Volume UP | | PL1 | |
| | VDW | Volume DOWN | | PL2 | |
| | DON | Display ON | | PL3 | |
| | DOF | Display OFF | | PL4 | |
| | MON | All Mute ON | | PL5 | |
| | MOF | All Mute OFF | | PS0 | |
| | AON | Audio Mute ON | | PS1 | |
| | AOF | Audio Mute OFF | | PS2 | |
| | FON | Freeze ON | | PS3 | |
| | FOF | Freeze OFF | | PS4 | |
| RGB | RON | Resize ON | | PS5 | |
| | ROF | Resize OFF | Mode | MW1 | Wide ON |
| Camera (for TLP511) | CFU | Focus UP | | MW0 | Wide OFF |
| | CFD | Focus DOWN | | MM1 | MIC ON |
| | CZU | Zoom UP | | MM0 | MIC OFF |
| | CZD | Zoom DOWN | | MO1 | OSD mute ON |
| Common adjustment | ALF | Menu left shift/ adjustment value DOWN | | MO0 | OSD mute OFF |
| | ARG | Menu right shift/ adjustment value UP | | PJ0 | Floor mounted front projection |
| | AUP | Menu up shift | | PJ1 | Ceiling mounted front projection |
| | ADW | Menu down shift | | PJ2 | Floor mounted rear projection |
| | RST | Standard setting for each item | | PJ3 | Ceiling munted rear projection |
| | SAV | Adjustment value storing | Language | LEN | English display |
| Video | VCN | Contrast | | LJP | Japanese display |
| | VBR | Bright | | LFR | French display |
| | VCL | Color | | LGR | German display |
| | VTN | Tint | | LSP | Spanish display |
| | VSH | Sharp | | LIT | Italian display |
| | | | Camera | CSH | High sensitivity ON |
| | | | | CSL | High sensitivity OFF |
| | | | | SIR | Iris adjustment |

# 6. DIGITAL CIRCUIT

## 6-1. Outline

A Configuration of digital circuit is shown in Fig. 6-1-1.
The functions of digital circuit are described on the following pages.

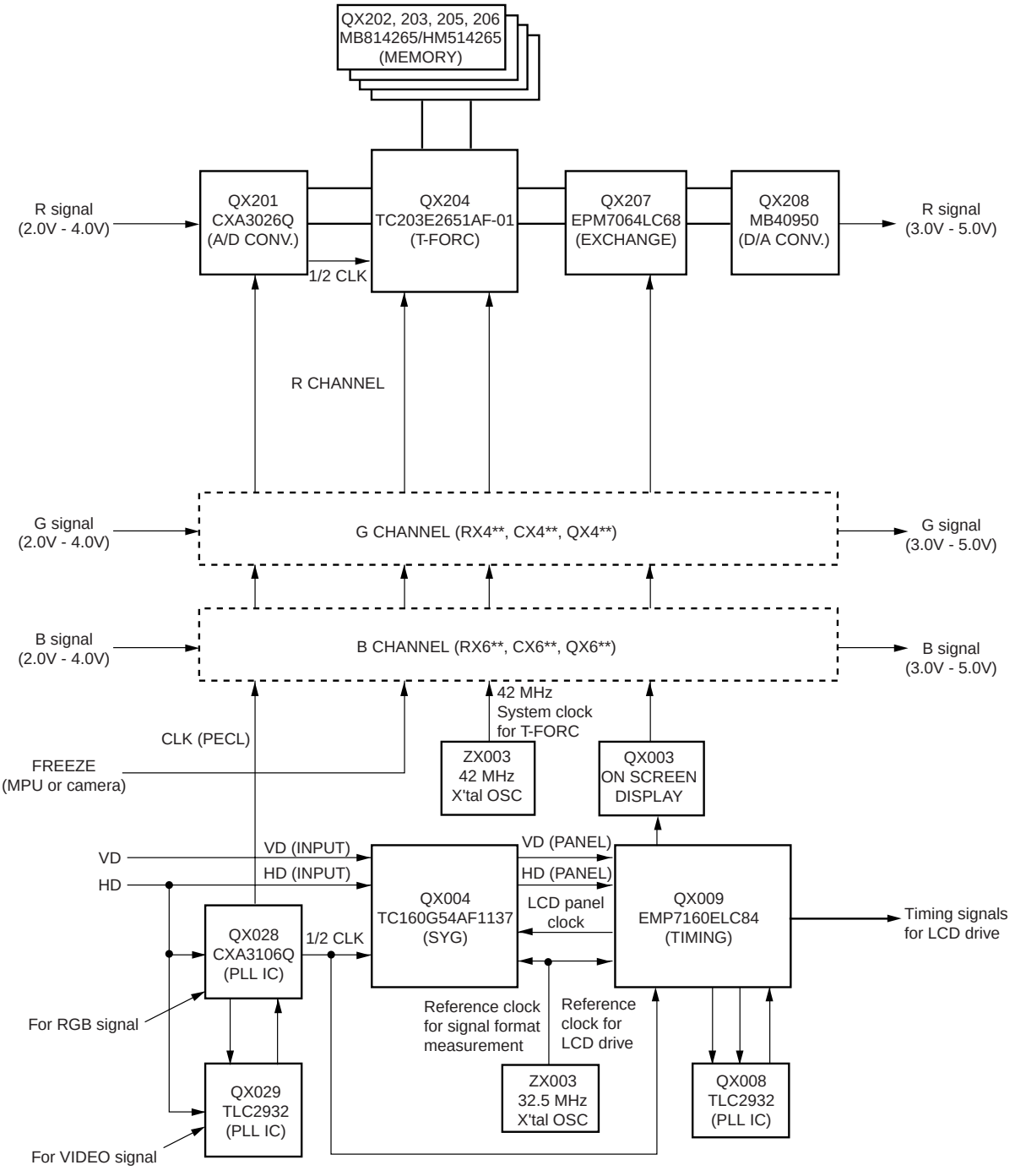



**Fig. 6-1-1**

### 6-1-1. PLL Circuit

The PLL circuit develops the clock signal synchronized with the horizontal sync signal, using the horizontal sync signal entered.

For RGB signals, a highly stable CXA3106 (QX028) is used. For video signal, a highly traceable TLC2932 (QX029) is used.

### 6-1-2. Video Signal Format Conversion

The LCD panel used for the unit requires a non-interlace signal of 65 Hz dot clock entered. Accordingly, all the RGB signals are converted into XGA 60 Hz format (Dot clock = 65 MHz). In the same way, the video signal (interlace signal) is converted into a non-interlace signal with 64 MHz dot clock in keeping the vertical sync signal frequency. These processes are carried out by the newly developed ICs T-FORC (QX207, QX407 and QX607) and memories (QX202, QX203, QX205, QX206, QX402, QX403, QX405, QX406, QX602, QX603, QX605 and QX606).

Furthermore, as the clock of XGA signal reaches approx. 80 MHz (max.), all signal processes are carried out in parallel for even and odd pixels grouped. The video signal entered is converted into the digital video signals for two systems by the A/D converters (QX204, QX401 and QX601).

The signals divided into two systems are processed in parallel in stages after the digital circuit. In case of the process carried out in parallel as described above, if the characteristics between two systems differ, the vertical stripes will appear on the screen. In order to reduce this vertical stripes, the signal system used is exchanged for every one line and one field by the EXCHANGE PLD (QX207, QX407 and QX607). The signals exchanged are returned to the original order just before reaching the LCD panel.

### 6-1-3. Screen Size Enlargement and Reduction

The pixel number of the LCD panel used for the unit is 1024 x 768 pixels. As for a signal entered, various kinds of signals are used ranging from 640 x 480 pixels of VGA signal to 1280 x 1024 pixels of SXGA signal. In this unit, these signals are displayed on the whole screen by enlarging/reducing the signals. The enlargement/reduction process are also carried out by the ICs T-FORC (QX207, QX407 and QX607) and memories (QX202, QX203, QX205, QX206, QX402, QX403, QX405, QX406, QX602, QX603, QX605 and QX606).

### 6-1-4. Gamma Correction Circuit

The gamma correction is carried out in the digital circuit. So the digital circuit develops the signal corrected in gamma.

The gamma correction circuit is built in the T-FORC (QX207, QX407 and QX607) and the gamma correction characteristics are set by the microprocessor using a bus.

### 6-1-5. Panel Driving Timing Signal Generation

The driving for LCD panel requires various kinds of timing signals. These timing signals are generated in the digital circuit and especially generated by the timing generation PLD (QX009).

### 6-1-6. ON-SCREEN Character Generation

The ON-SCREEN character timing signal is generated and superimposed inside the digital circuit. So the signal composed of the ON-SCREEN character is developed from the digital circuit.

### 6-1-7. Signal Format Measurement

The RGB signals consist of various kinds of signal formats, and the timing signal, enlargement ratio and etc. must be switched corresponding to each signal format.

For this purpose, the signal format identification is carried out by measuring the HD signal frequency entered and the line number per 1 frame. This circuit is built in the SYG (QX004) and the processed result is read by the microprocessor through the bus line.

## 6-2. Each IC Description

### 6-2-1. PLL IC CXA3106Q (QX028) for RGB Signals

A configuration of CXA3106Q is shown in Fig. 6-2-1. The PLL IC of CXA3106Q is an IC with high performance and low jitter, and can generate the clock signal synchronized with the horizontal sync signal of max. 120 MHz.

The VCO, phase comparator, loop filter and frequency dividing circuit are built in the IC, so the IC can generate the clock signal by itself.

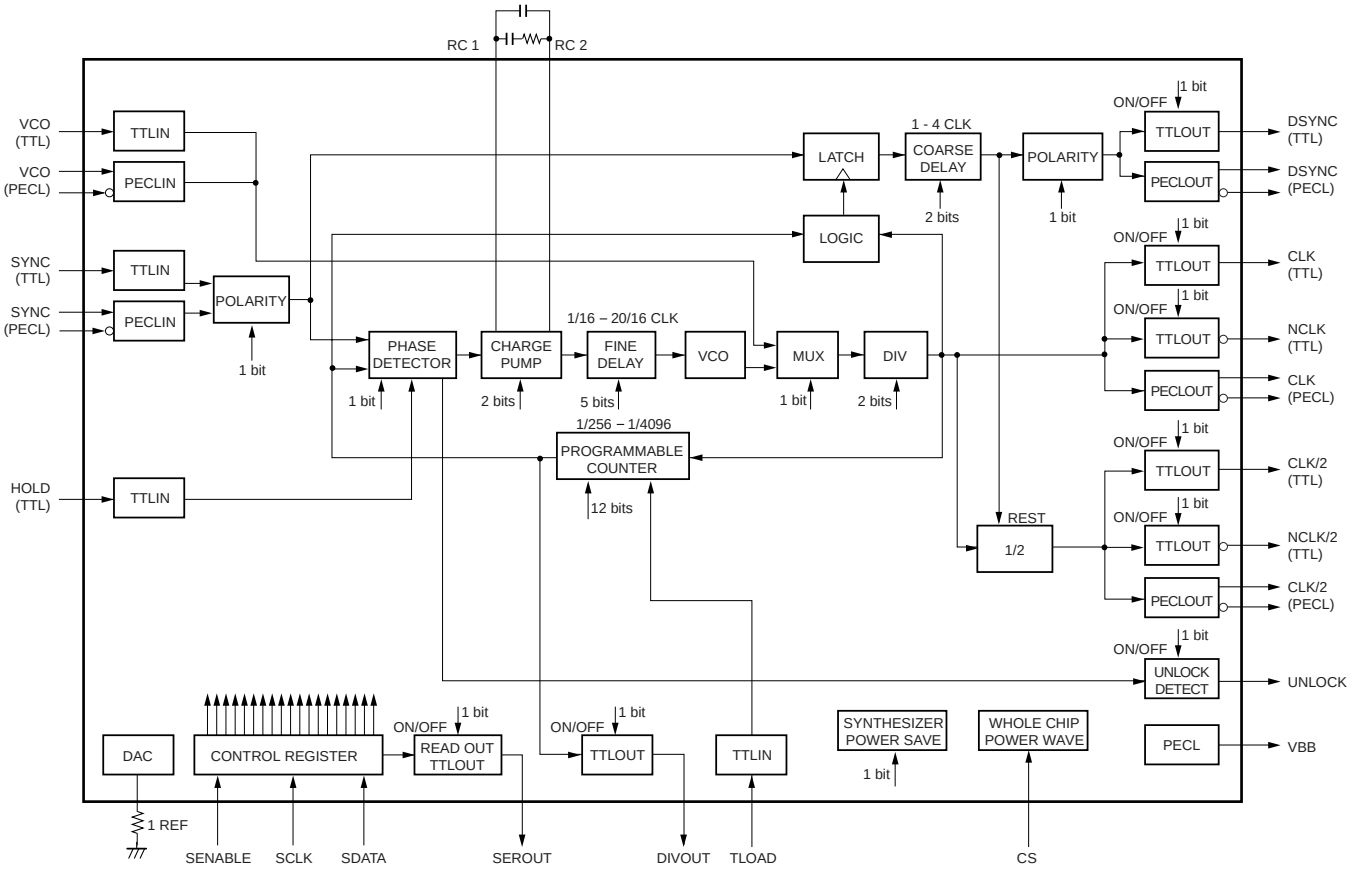



**Fig. 6-2-1**

### 6-2-2. PLL IC TLC2932 (QX029) for Video Signal

The PLL IC of TLC2932 is composed of a phase comparator and a VCO. As a frequency dividing circuit is not built in, so the IC works as a PLL circuit by connecting to the external VCO terminal of QX028 and using the frequency dividing circuit of QX028.

### 6-2-3. Sync Process IC SYG (QX004)

A configuration of the SYG component is shown in Fig. 6-2-2. The SYG IC is used as a sync process IC and composed of the timing generation circuit for 2 systems, one for the input signal and the other is for the panel display, and the input signal measurement circuit. The IC supplies the HD/VD signal to each IC and the IC works on the timing signal basis. Also, the field identification at video signal is carried out by the IC. In the unit, as the PLL circuit is independent from the SYG, the sync signal (DSYNC) enters from the PLL circuit to pin 139. The pin is connected to the reset terminal of the horizontal counter (for input signal).

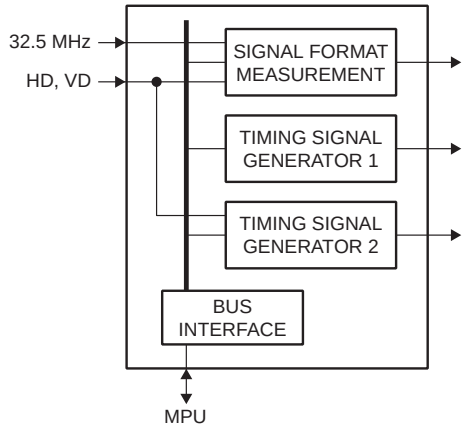



**Fig. 6-2-2**

### 6-2-4. Timing Signal Generation PLD (QX009)

A configuration of timing signal generation PLD is shown in Fig. 6-2-3. The timing generation PLD generates the clock pulse and the timing signal to drive the panel. As the signal timing and clock differ owing to the inverted driving for top/bottom/left/right of panel and kinds of input signals, the mode signal controls the timing signal generation PLD.

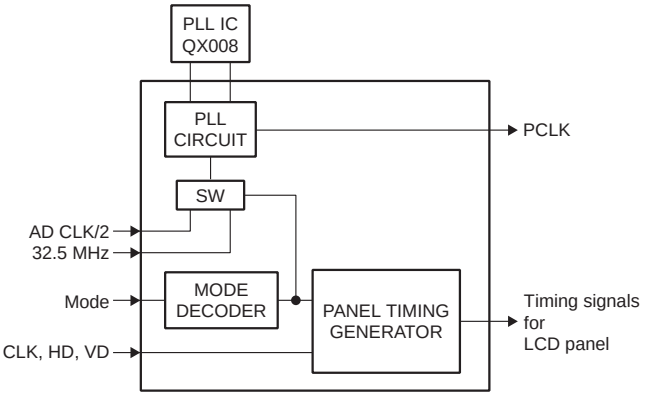



**Fig. 6-2-3**

### 6-2-5. A/D Converter CXA3026Q (QX201, QX401 and QX601)

A configuration of CXA3026Q is shown in Fig. 6-2-4. The max. conversion speed of 120 MHz is supported by CXA3026Q, A/D converter.

A frequency dividing circuit is built in the A/D converter and the converter develops the data for two systems. The clock speed is fast, so that the clock signal to be entered is a differential input of PECL level. The input level of analog signal ranges from 2.0 to 4.0V.

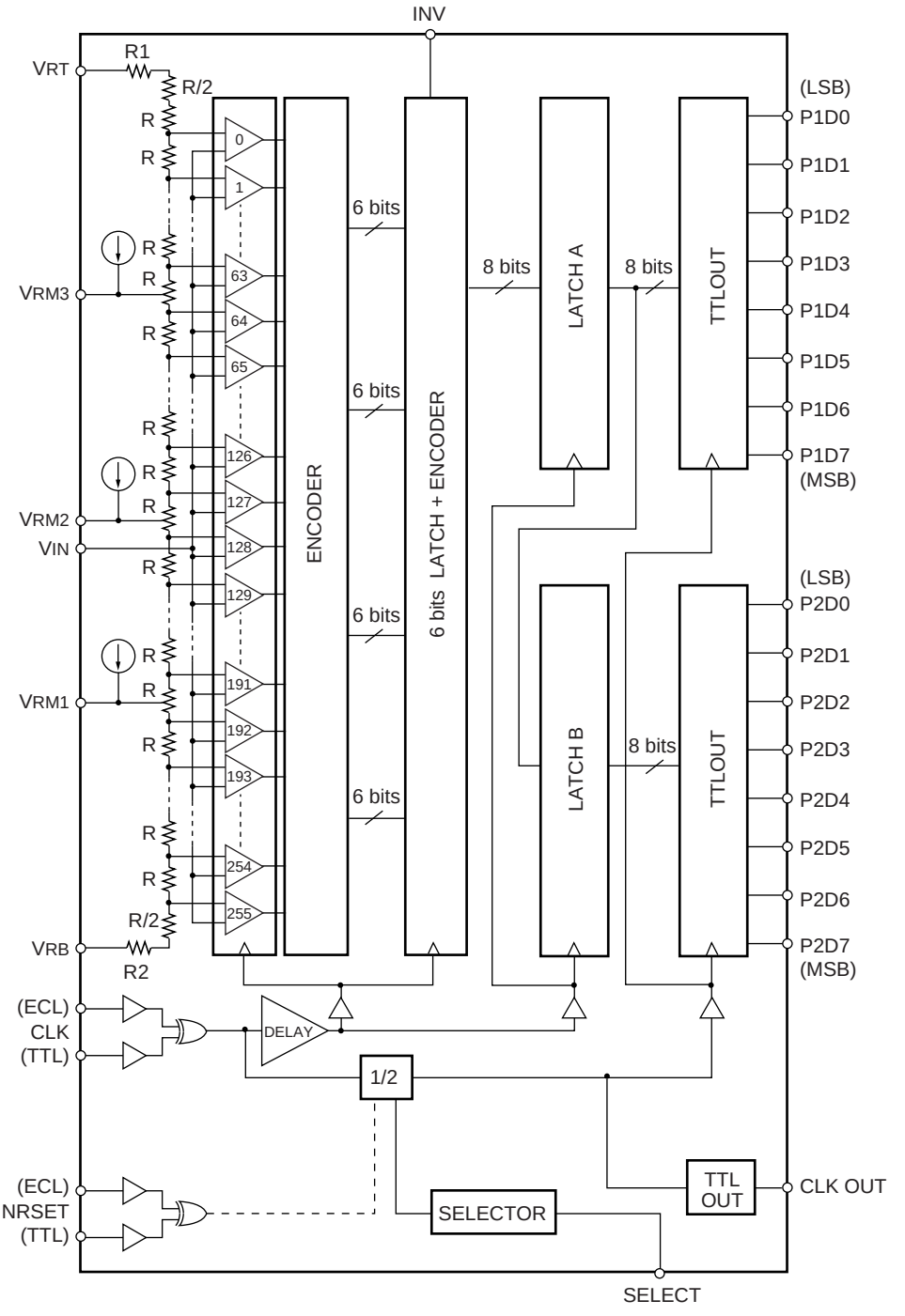

INV
VRT
R1
R/2
R
R
0
1
6 bits
8 bits
LATCH A
8 bits
TTLOUT
(LSB)
P1D0
P1D1
P1D2
P1D3
P1D4
P1D5
P1D6
P1D7
(MSB)
VRM3
63
64
65
126
127
VRM2
VIN
128
129
ENCODER
6 bits LATCH + ENCODER
191
VRM1
192
193
254
255
R/2
VRB
R2
LATCH B
8 bits
TTLOUT
(LSB)
P2D0
P2D1
P2D2
P2D3
P2D4
P2D5
P2D6
P2D7
(MSB)
(ECL)
CLK
(TTL)
DELAY
1/2
(ECL)
NRSET
(TTL)
SELECTOR
TTL
OUT
CLK OUT
SELECT

**Fig. 6-2-4**

### 6-2-6. Picture Size of View Conversion IC T-FORC (QX204, QX404, QX604)

A configuration of T-FORC is shown in Fig. 6-2-5. The T-FORC is a newly developed picture size conversion IC.

By using the IC, smooth picture enlargement and reduction, and format conversion will be made. Also, a gamma correction circuit is built in the IC.

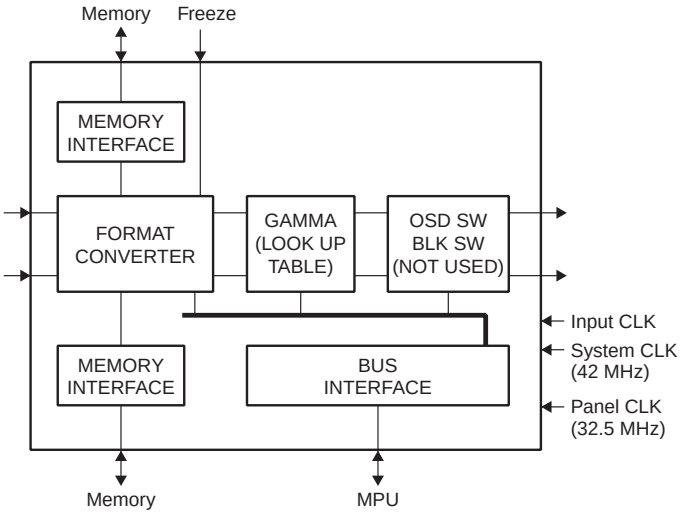



**Fig. 6-2-5**

### 6-2-7. Memory

The memory uses four general 4 M bits EDO-DRAMs (256k **x** 16 bits) per 1 channel.

### 6-2-8. Exchange PLD

A configuration of timing signal generation PLD is shown in Fig. 6-2-6. In the unit, the signal process is carried out in parallel by dividing the process into two systems. In order to reduce the characteristic difference between these two systems, the signals of both systems are switched for every 1 line and 1 frame. The PLD carries out the process. Also, the ON-SCREEN display signal superimposing, addition of non-display section for top and bottom and left and right, etc. are carried out by the PLD.

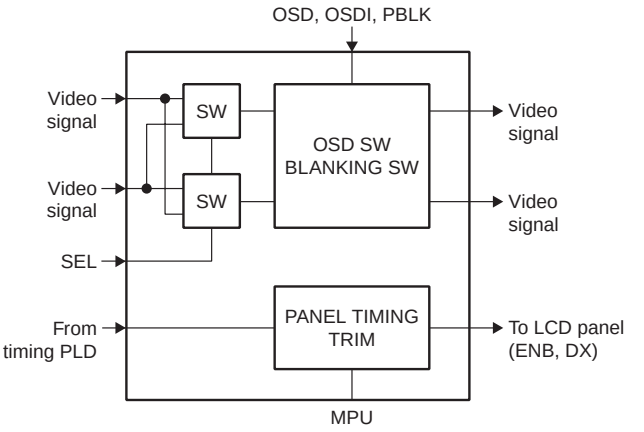



**Fig. 6-2-6**

### 6-2-9. D/A Converter

MB40950 is a 10 bits 3 channels D/A converter of which max. conversion speed is 60 MHz. In order to reduce the difference of two systems of each RGB channel, each RGB channel possesses one IC respectively. So one channel of 3 channels D/A converter built in the IC is not used. The output signal level ranges from 3.0 to 5.0V.

# 7. VIDEO CIRCUIT

## 7-1. Circuit Component

The video circuit performs selection of input signals, video signal (NTSC, PAL, SECAM) demodulation to RGB signals, RGB input signal amplification and audio signal amplification.

Fig. 7-1-1 shows the block diagram.

### 7-1-1. Input Signal SW Section

**<Video input section>**

All the video and audio signals entered are sent to the input SW IC (except for RGB signals). In the input SW IC, the signals are switched corresponding to the composite, Y/C and color modes (NTSC, PAL SECAM and BLACK & WHITE) respectively. Processing routes for the composite video signals are changed depending on the color modes (NTSC, PAL, SECAM and BLACK & WHITE). Y/C signals, SECAM and Black & White signals are supplied to the video color process IC in the next stage passing through the input SW IC. NTSC, PAL and 4.43 NTSC color signals only are separated into the luminance Y signal and color C signal by the digital comb filter and then enter the input SW IC again as the Y/C signals.

In the cases other than described above, when the power is on or the input switching occurs, the signals are supplied to the video/color process IC as a composite video signal passing through the input SW IC.

**<RGB input section>**

The RGB signals entered are divided in two systems; the internal signal process and external output systems.

The signals for the external output system enter 75 ohm driver IC and then enter D-sub 15 pin for output. The RGB signals for internal signal process system enter the mute IC. When the video signal is selected, the RGB signals are muted by the mute IC output.

### 7-1-2. Video Demodulation Section

In the video demodulation section, the composite video signal and Y/C signals are demodulated into the RGB signals.

In the video/color process IC, the color demodulation is carried out corresponding to the color mode of the video signal entered. The applicable color modes are NTSC, 4.43 NTSC, PAL and SECAM.

The mode identification is automatically carried out by the video/color process IC.

When the power turns on and the input is switched, the composite video signal passing through the input SW IC enters and the color mode is determined. The microprocessor detects the result of color mode determination and sets a corresponding color mode. The color difference signal demodulated by the video/color process IC is developed after processed its phase and signal level via 1H delay IC.

The luminance signal enters the picture quality correction IC and the color difference signal enters the RGB demodulation IC via the delay line for matching with the luminance signal.

In the RGB demodulation IC, the gamma correction, color adjustment, etc. are carried out as well as the luminance color difference signal is demodulated to the RGB signals.

### 7-1-3. RGB Signal Amplification Section

In the RGB signal amplification section, the RGB input signals and the video signal demodulated to the RGB signals are switched and the contrast and brightness adjustments are carried out. Further, the gain adjustment for each RGB signal is also carried out.

The sync signals of the RGB signals correspond to HD,VD, composite sync (CS) and SYNC ON G signals.

### 7-1-4. Audio Signal Amplification Section

The audio signal inputs of the video and RGB inputs correspond to L and R stereo input. After switching the input, the signal develops at the audio terminal through the output buffer circuit. After L and R signals are mixed, the sound volume control IC controls its level, thus controlled signal is amplified to the sufficient level to drive the speaker by the audio output IC, and then sent to the speaker.

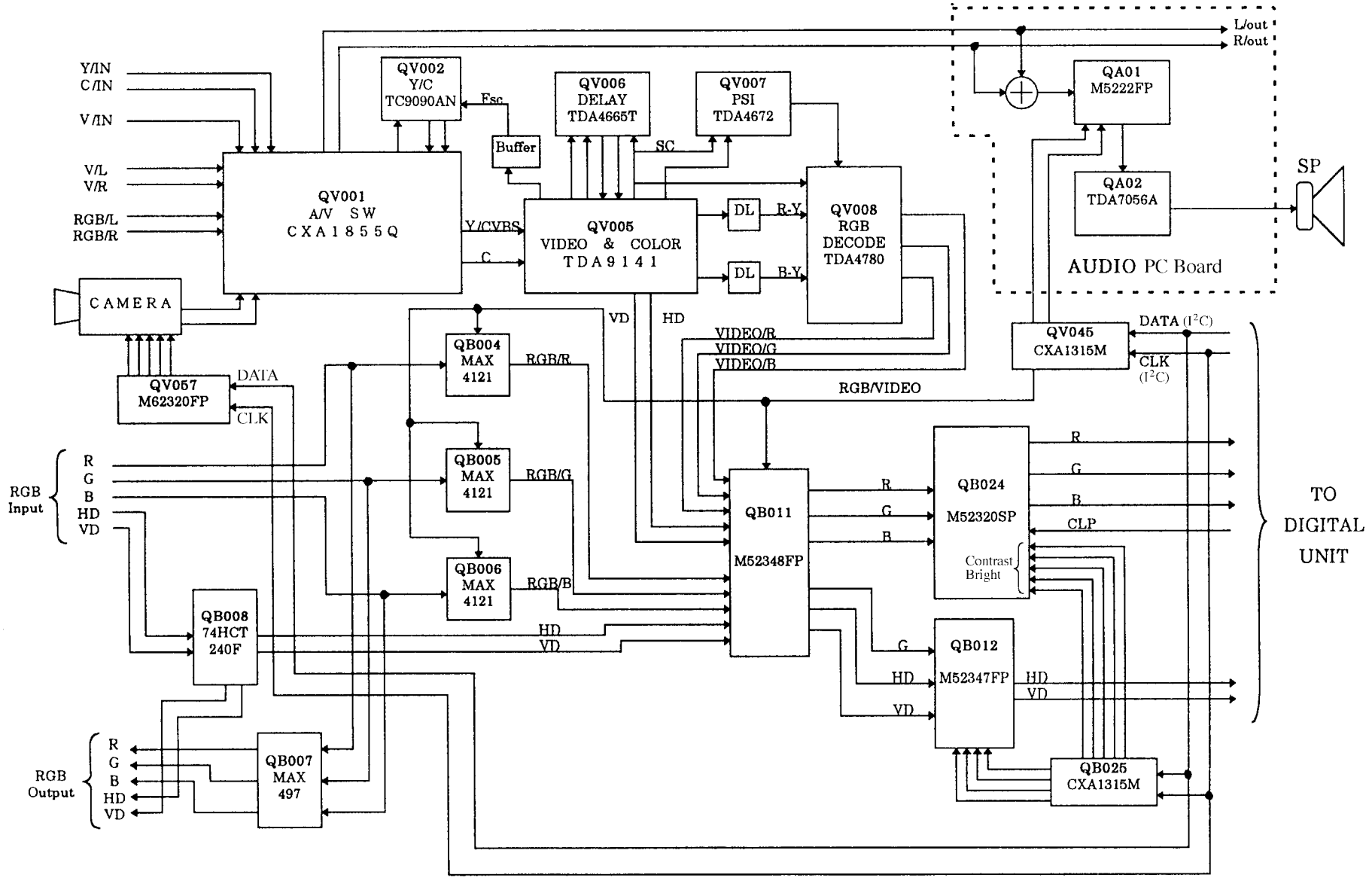



**Fig. 7-1-1 Block diagram**

## 7-2. Input Signal Switch Section

The signal SW section works as a circuit to supply the signal to the signal process section in the next stage and each output terminal by switching the signal entered (video, audio).

Each input signal is sent to QV001 (CXA1855Q) as shown in Fig. 7-2-1. The IC control is carried out by $I^2C$ bus.

### 7-2-1. Video Signal

The composite video signal enters pins 43 (V1) and 45 (Y1) at the same time. When the composite signal entered is a NTSC/PAL color signal, pin 43 (V1) is selected. When it is either a SECAM or Black & White signal and when the input switching is carried out, pin 45 (Y1) is selected.

This is because the composite signal is supplied to the video/color process IC in the next stage passing through the Y/C separation IC QV002 (TC9090AN) when the composite signal is either SECAM or black & white signal and when the input switching is carried out.

This is also because in the Y/C separation IC QV002 (TC9090AN), the SECAM signal cannot be separated into Y and C signals, and it is not necessary for the Black & White signal to be separated in Y and C signals.

The signal developed from pin 34 is Y/C-separated by Y/C separation IC QV002 (TC9090AN) and then enters the signal SW IC QV001 (CXA1855Q) again. (Pin 31 (Y), pin 29 (C))

The Y/C signals entered from S terminal enter pins 3 and 5 respectively.

In case of TLP511, the video signal from the camera section is supplied as Y/C signals and enters pins 9 and 11 respectively.

The video signal selected finally develops from pins 37 (Y) and 29 (C) respectively.

### 7-2-2. Audio Signal

The audio signal employs two input systems; one is for video signal and the other is for RGB signals. Each system is applicable to L and R stereo inputs respectively.

The audio signal for the video signal is selected when the video signal is selected and the audio signal for RGB signals is selected when the RGB signals are selected.

The audio signal selected develops from pins 33 (L) and 32 (R).

### 7-2-3. RGB Signal

The RGB signals are entered using a high density D-SUB 15 and separated in two systems for the internal signal process and the external output signal. The external output signal develops at PV002 (RGB output connector) via QB007 (6 dB amp.). When the power turns on, the RGB output signals always develop if any signal enters at the RGB input terminal.

On the other hand, the internal process signals for the RGB signals enter QB004, QB005 and QB006, respectively. The input signal switch IC controls to mute the RGB input signals when selecting the video input.

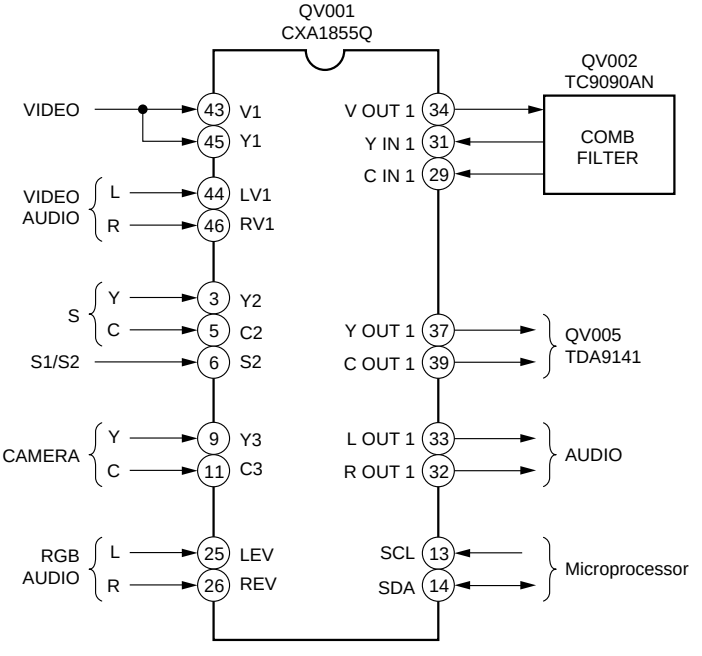



**Fig. 7-2-1**

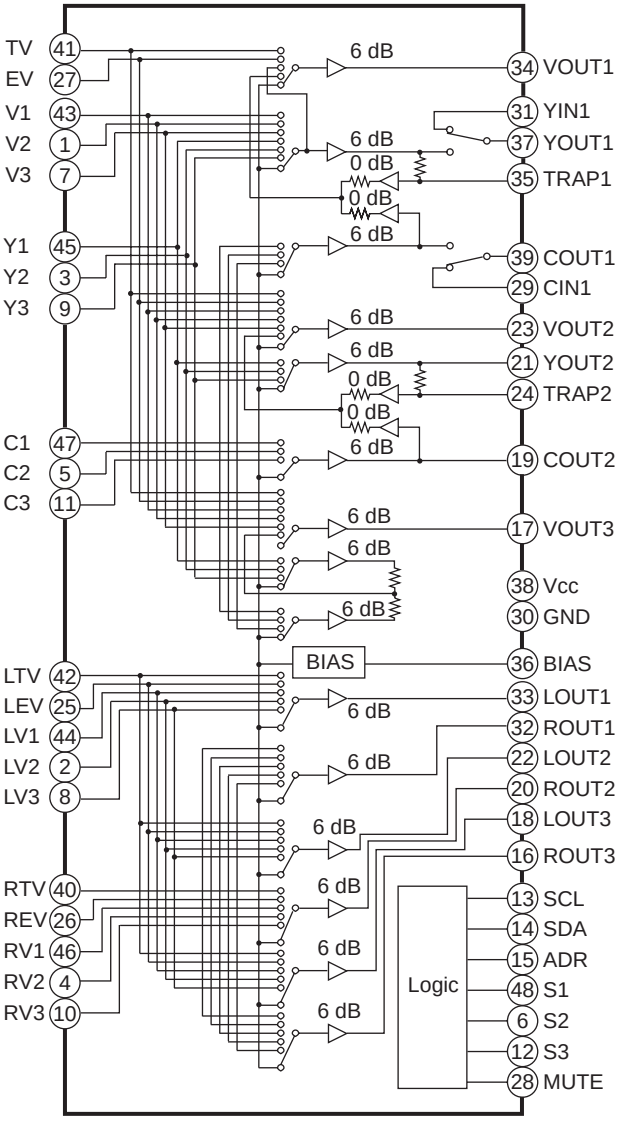



**Fig. 7-2-2 Internal block diagram of CXA1855Q**

## 7-3. Video Demodulation Block

### 7-3-1. Y/C Separation Circuit

This circuit separates Y and C signals from a composite video signal. Fig. 7-3-1 shows the pin configuration of TC9090AN and Fig. 7-3-2 shows the block diagram.

The composite video signal enters pin 3. A fsc (3.58/4.43 MHz) developed from the video/color IC enters pin 19 and is converted into a 4fsc of the drive clock frequency inside the IC. The composite video signal entered is processed at a rate of the clock frequency of the IC and output as Y and C signal.

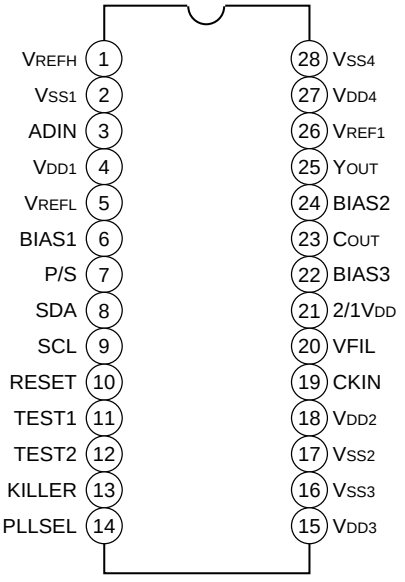



**Fig. 7-3-1 Pin configuration of TC9090AN**

**Table 7-3-1 Terminal function of TC9090AN**

| Pin No. | Name | Function |
|---|---|---|
| 1 | $V_{REFH}$ | ADC bias |
| 2 | $V_{SS1}$ | ADC GND |
| 3 | ADIN | Video input |
| 4 | $V_{DD1}$ | ADC VDD |
| 5 | $V_{REFL}$ | ADC bias |
| 6 | BIAS1 | ADC bias |
| 7 | P/S | Selection function control |
| 8 | SDA | $I^2C$ bus clock input |
| 9 | SCL | $I^2C$ bus data input, check output |
| 10 | RESET | $I^2C$ bus reset |
| 11 | TEST1 | Test terminal |
| 12 | TEST2 | Test terminal |
| 13 | KILLER | Clock killer switch |
| 14 | PLLSEL | Selection input clock |
| 15 | $V_{DD3}$ | Digital VDD |
| 16 | $V_{SS3}$ | Analog GND |
| 17 | $V_{SS2}$ | PLL GND |
| 18 | $V_{DD2}$ | PLL VDD |
| 19 | CKIN | Clock input |
| 20 | VFIL | VCO filter |
| 21 | 2/1 $V_{DD}$ | Line memory bias |
| 22 | BIAS3 | DAC bias |
| 23 | $C_{OUT}$ | C output |
| 24 | BIAS2 | DAC bias |
| 25 | $Y_{OUT}$ | Y output |
| 26 | $V_{REF1}$ | DAC bias |
| 27 | $V_{DD4}$ | DAC VDD |
| 28 | $V_{SS4}$ | DAC GND |

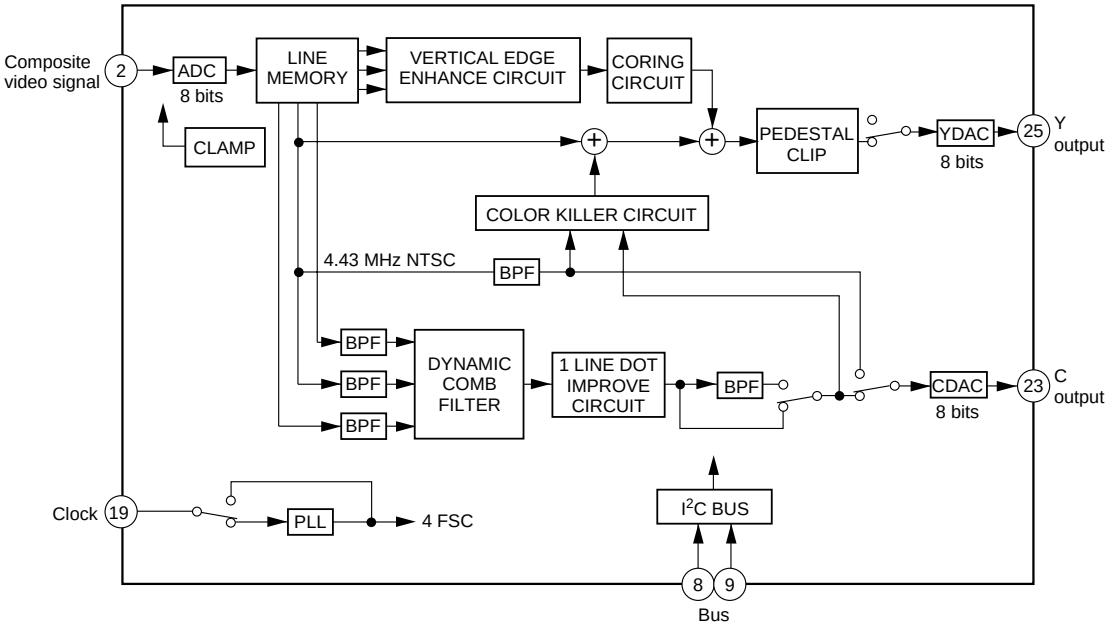



**Fig. 7-3-2 Block diagram of TC9090AN**

### 7-3-2. Video/Color Circuit

The video/color circuit consists of two ICs, QV005 (TDA9141: NTSC/PAL/SECAM DECODER), QV006 (TDA4665T: BASE BAND DELAY LINE), and supports each system of NTSC, PAL and SECAM.

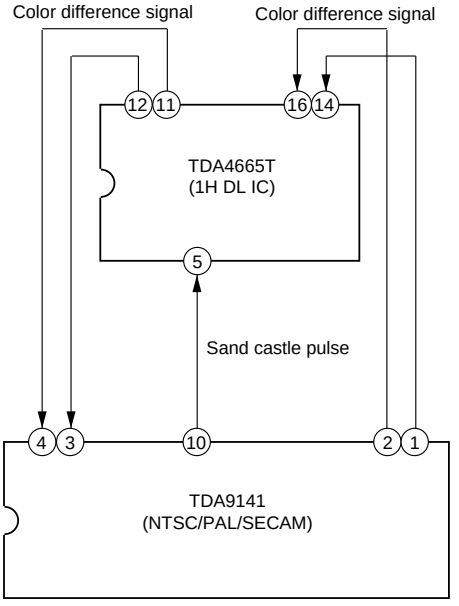



**Fig. 7-3-3**

Fig. 7-3-4 shows the pin configuration of TDA9141 and Fig. 7-3-5 shows the block diagram of TDA9141. Fig. 7-3-6 shows the pin configuration of TDA4665T and Fig. 7-3-7 shows the block diagram of TDA4665T.

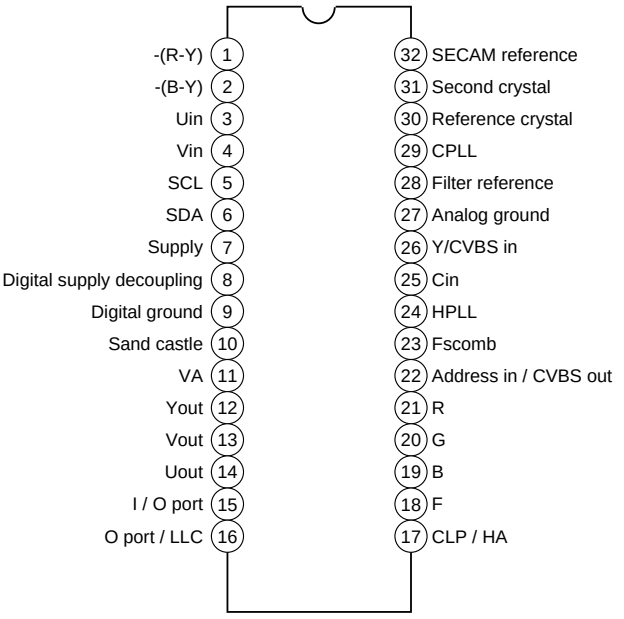



**Fig. 7-3-4 Pin configuration of TDA9141**

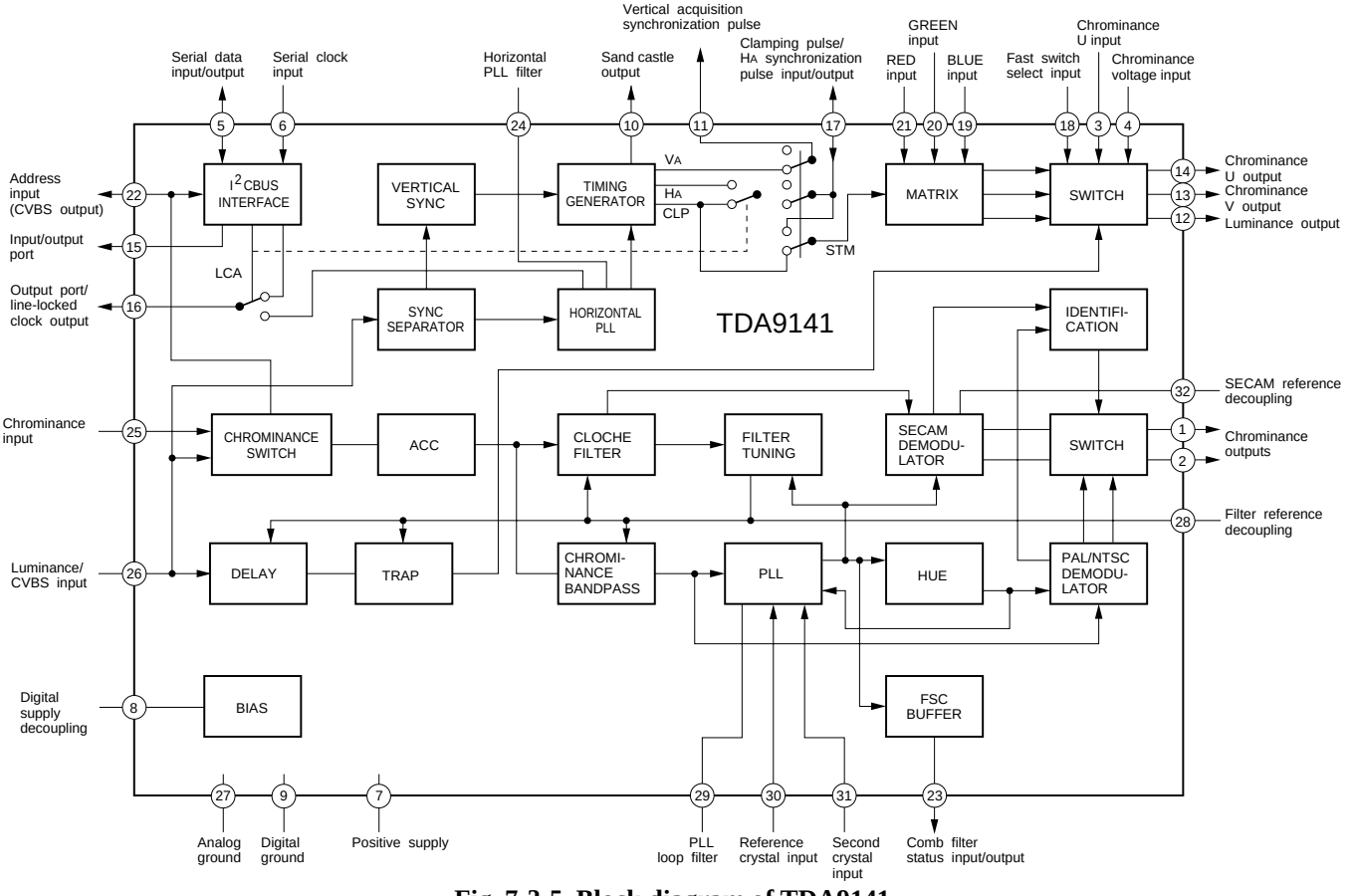



**Fig. 7-3-5 Block diagram of TDA9141**

TDA9141 has two input terminals for the composite video/Y signal (pin 25) and C signal (pin 26), and each of the signals is automatically identified through I$^2$C-BUS control.

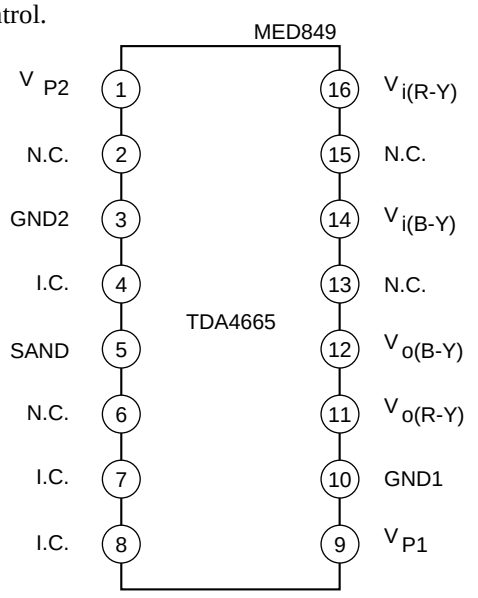



**Fig. 7-3-6 Pin configuration of TDA4665T**

**Table 7-3-2 Terminal function of TDA4665T**

| Pin No. | Name | Function |
|---|---|---|
| 1 | $V_{P2}$ | +5V power supply for digital block |
| 2 | N.C. | Not used |
| 3 | GND2 | GND (0V) for digital block |
| 4 | I.C. | Internal connection |
| 5 | SAND | Sandcastle pulse input |
| 6 | N.C. | Not used |
| 7 | I.C. | Internal connection |
| 8 | I.C. | Internal connection |
| 9 | VP1 | +5V power supply for analog block |
| 10 | GND1 | GND (0V) for analog block |
| 11 | $V_{o(R-Y)}$ | ± (R–Y) output signal |
| 12 | $V_{o(B-Y)}$ | ± (B–Y) output signal |
| 13 | N.C. | Not used |
| 14 | $V_{i(B-Y)}$ | ± (B–Y) input signal |
| 15 | N.C. | Not used |
| 16 | $V_{i(R-Y)}$ | ± (R–Y) input signal |

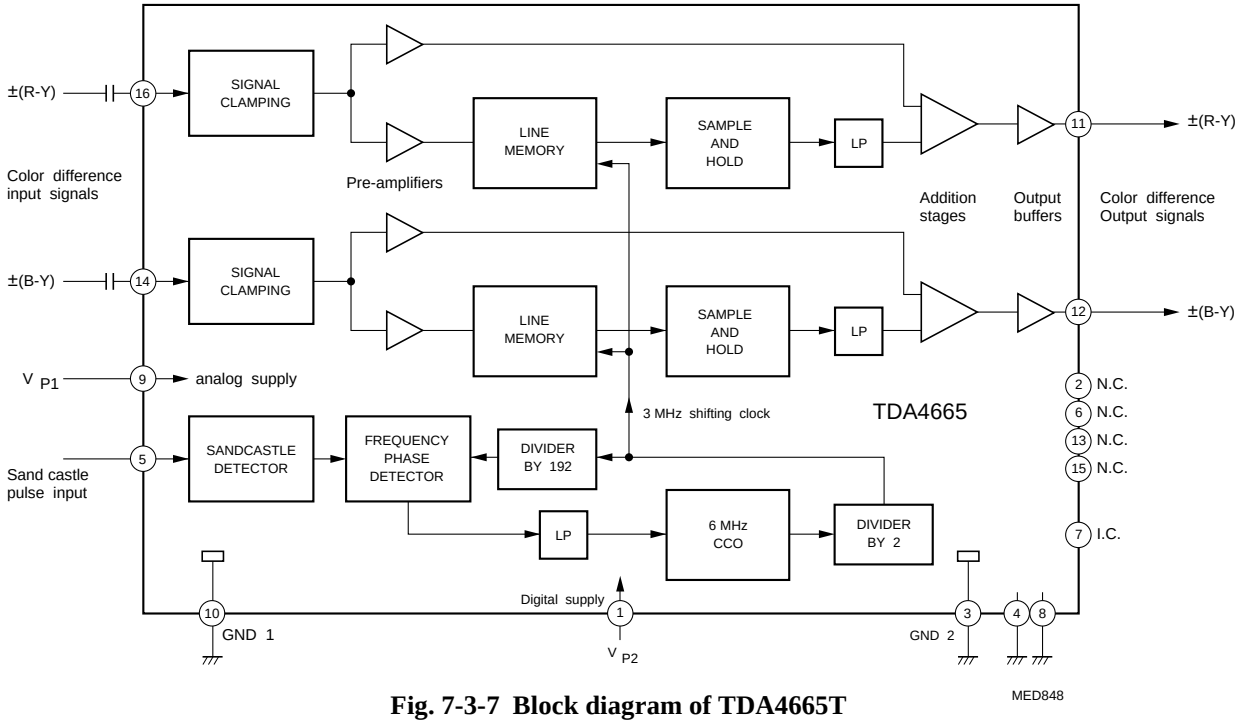



**Fig. 7-3-7 Block diagram of TDA4665T**

### 7-3-3. Luminance (Y) Signal Process Circuit

The processing method differs as follows depending on type of the signal entered.

(a) For a SECAM input, it passes through a burst signal trap circuit.

(b) For a NTSC/PAL (with burst signal) input (Y/C-separated signals), the burst signal trap circuit is bypassed. It passes through a delay circuit for a phase matching to the color signal.

(c) For a NTSC/PAL (without burst signal) input, above trap circuit and the delay circuit are bypassed to perform a stable color killer operation.

### 7-3-4. Color Signal Process Circuit

The color signal is level adjusted in the ACC (automatic color control) circuit, corrected in passing through a band pass circuit in the NTSC/PAL system, or a bell filter correction is carried out in the SECAM system, and then enters the color demodulation circuit.

The input burst signal is locked with a crystal oscillator frequency (3.58 MHz/4.43 MHz) in the PLL circuit and then demodulated into color difference signals after a tint adjustment (in the NTSC system). The demodulation for the SECAM signal is carried out using a PLL circuit.

The demodulated color difference signals are output through low pass filters, delayed by 1H in passing through TDA4665T, fed to TDA9141 again and directly output.

### 7-3-5. Picture Sharpness Correction Circuit

The picture sharpness is carried out by QV007, TDA4672. Fig. 7-3-8 shows the pin configuration of TDA4672 and Fig. 7-3-9 shows the block diagram.

Picture sharpness correction frequency is set to 2.6 MHz.

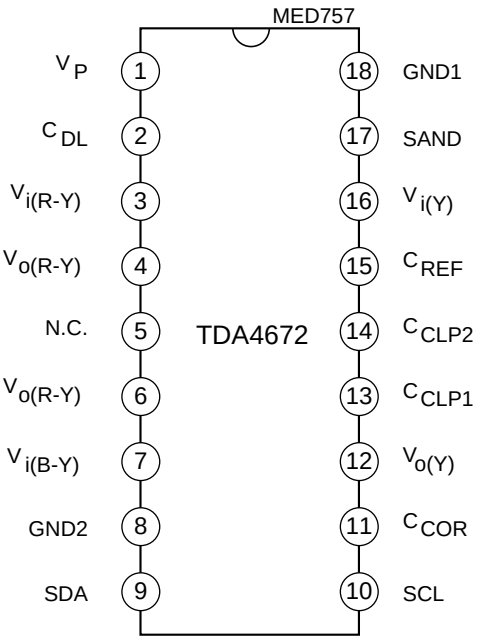



**Fig. 7-3-8 Pin configuration of TDA4672**

**Table 7-3-3 Terminal function of TDA4672**

| Pin No. | Name | Function |
|---|---|---|
| 1 | $V_P$ | Positive power supply |
| 2 | $C_{DL}$ | Capacitor for delay time control |
| 3 | $V_{i(R–Y)}$ | ± (R–Y) color difference input signal |
| 4 | $V_{o(R–Y)}$ | ± (R–Y) color difference output signal |
| 5 | N.C. | Not used |
| 6 | $V_{o(B–Y)}$ | ± (B–Y) color difference output signal |
| 7 | $V_{i(B–Y)}$ | ± (B–Y) color difference input signal |
| 8 | GND2 | GND 2 (0V) |
| 9 | SDA | $I^2C$ bus data line |
| 10 | SCL | $I^2C$ bus clock line |
| 11 | $C_{COR}$ | Magnetic core capacitor |
| 12 | $V_{o(Y)}$ | Delay luminance output signal |
| 13 | $C_{CLP1}$ | Black level clamp capacitor 1 |
| 14 | $C_{CLP2}$ | Black level clamp capacitor 2 |
| 15 | $C_{REF}$ | Reference voltage capacitor |
| 16 | $V_{i(Y)}$ | Luminance input signal |
| 17 | SAND | Sandcastle pulse input |
| 18 | GND1 | GND 1 (0V) |

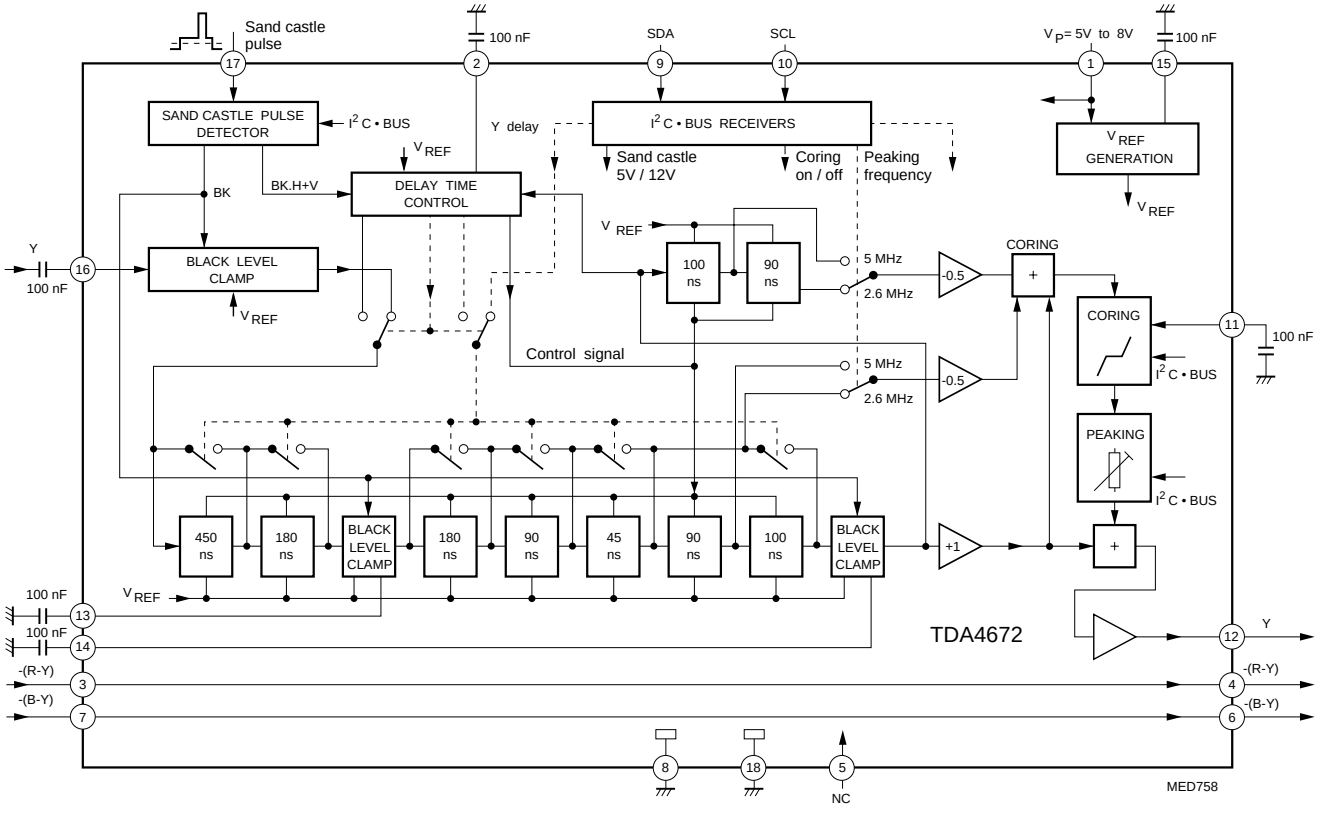



**Fig. 7-3-9 Block diagram of TDA4672**

### 7-3-6. RGB Demodulation

The demodulation from Y and color difference signals to RGB signals is carried out by QV008, TDA4780. Fig. 7-3-10 shows the pin configuration of TDA4780 and Fig. 7-3-11 shows the block diagram. The TDA4780 performs the RGB demodulation and adjusts color, contrast, and brightness.

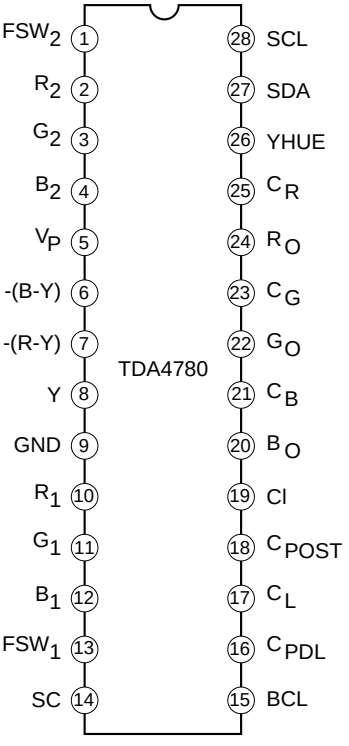



**Fig. 7-3-10 Pin configuration of TDA4780**

**Table 7-3-4 Terminal function of TDA4780**

| Pin No. | Name | Function | Pin No. | Name | Function |
|---|---|---|---|---|---|
| 1 | $FSW_2$ | High speed switch 2 input | 15 | BCL | Equal beam current limit input |
| 2 | $R_2$ | Red input 2 | 16 | $C_{PDL}$ | Memory capacitor for peak limit |
| 3 | $G_2$ | Green input 2 | 17 | CL | Memory capacitor for leakage current compensation |
| 4 | $B_2$ | Blue input 2 | 18 | $C_{POST}$ | Memory capacitor for peak dark |
| 5 | $V_P$ | Power supply voltage | 19 | CI | Cut-off measurement input |
| 6 | –(B–Y) | Color difference input – (B–Y) | 20 | $B_O$ | Blue output |
| 7 | –(R–Y) | Color difference input – (R–Y) | 21 | $C_G$ | Blue cut-off memory capacitor |
| 8 | Y | Luminance input | 22 | $G_O$ | Green output |
| 9 | GND | GND | 23 | $C_G$ | Green cut-off memory capacitor |
| 10 | $R_1$ | Red input 1 | 24 | $R_O$ | Red output |
| 11 | $G_1$ | Green input 1 | 25 | $C_R$ | Red cut-off memory capacitor |
| 12 | $B_1$ | Blue input 1 | 26 | YHUE | Y output/hue adjustment output |
| 13 | $FSW_1$ | High speed switch 1 input | 27 | SDA | $I^2C$ bus serial data input/check output |
| 14 | SC | Sandcastle pulse input | 28 | SCL | $I^2C$ bus serial clock input |

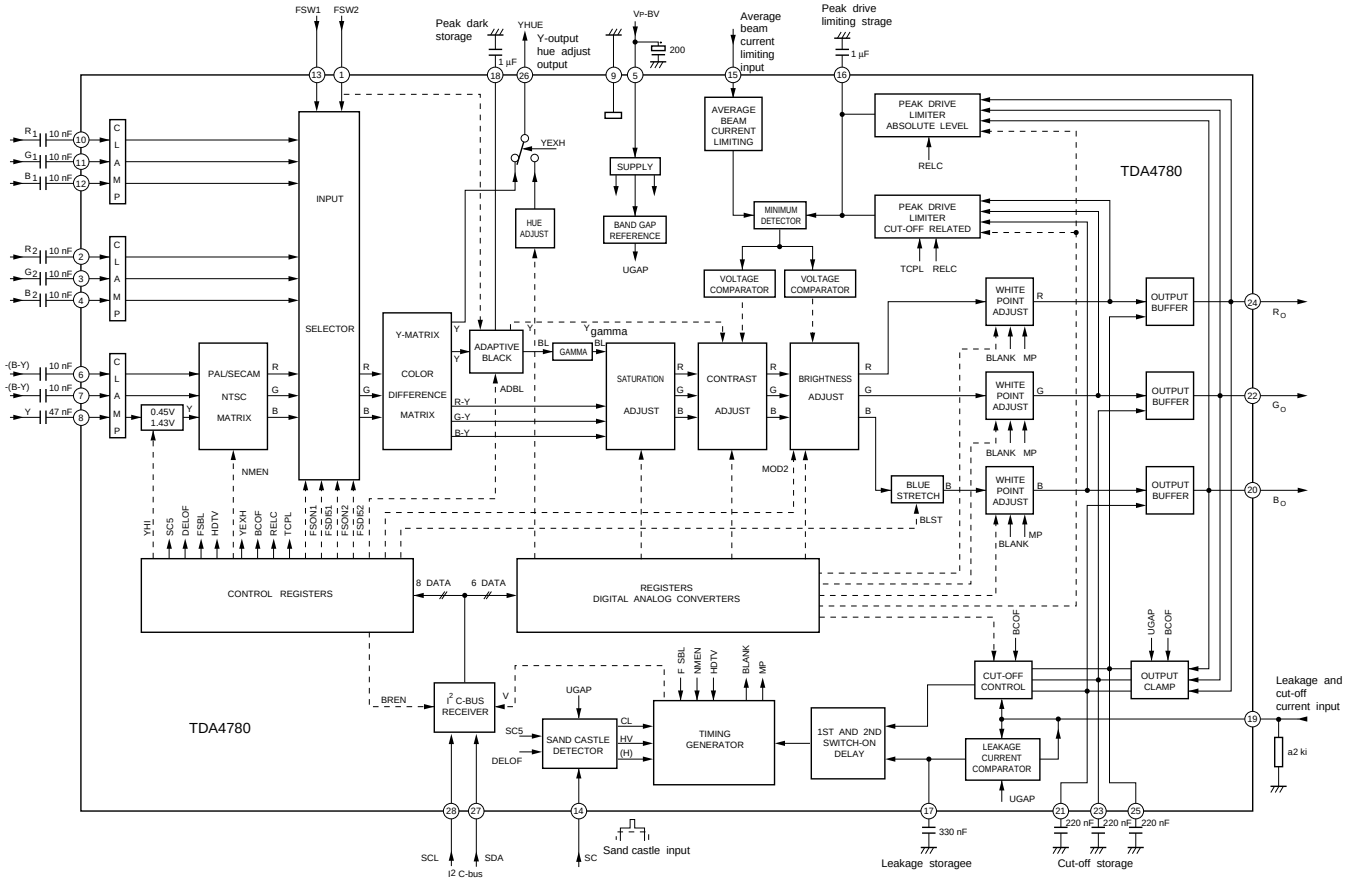



**Fig. 7-3-11 Block diagram of TDA4780**

### 7-3-7. Audio Circuit

Fig. 7-3-12 shows the audio circuit block diagram.

Signal path from the QV001 to the LINE OUT terminal is: QV001 ® transistor buffer ® LINE OUT terminal.

Signal path from the QV001 to the speaker is as follows. The audio signal developed from the QV001 becomes one signal with its L and R signal components mixed. The mixed audio signal enters the electrical volume IC QA01 (M5222FP) and the output level is controlled within a range of about 0 dB to –80 dB by an external DC voltage (DAC). The audio signal thus controlled by the IC QA01 is fed to the speaker amplifier IC QA02 (TDA7056A) and amplified by about 36 dB to drive the speaker.

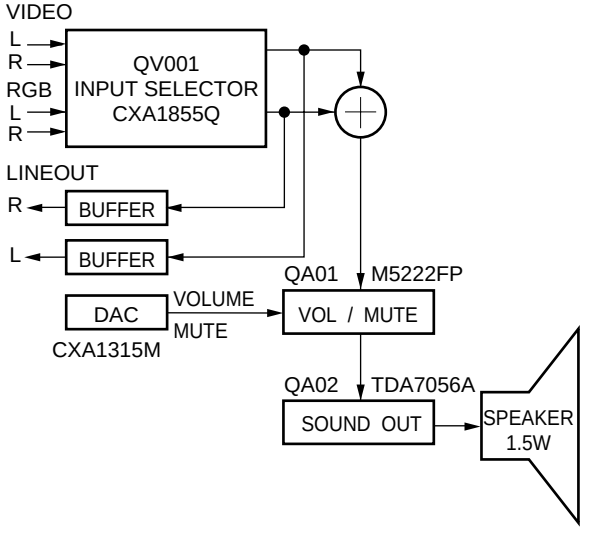
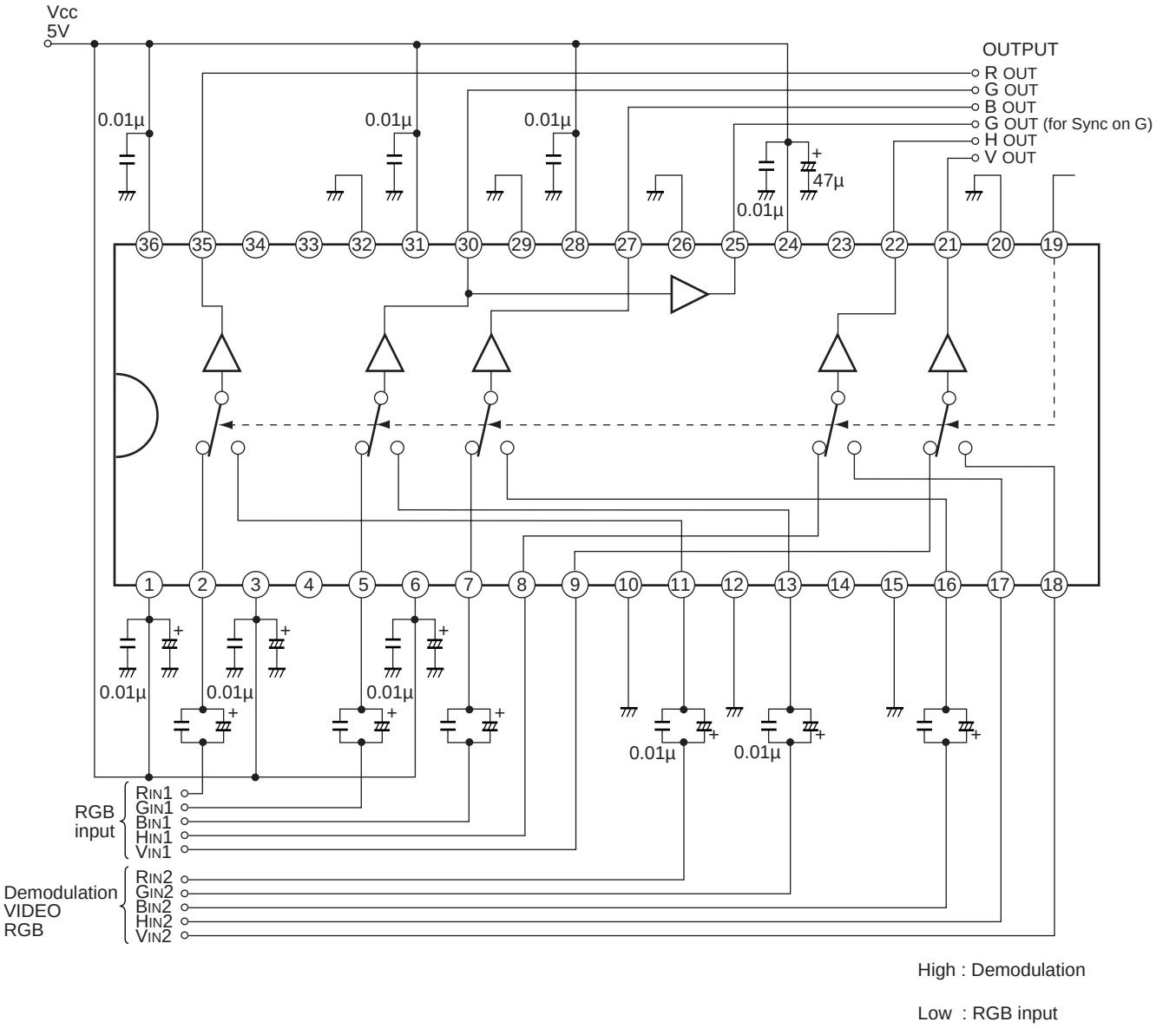



**Fig. 7-3-12 Audio circuit block diagram**

## 7-4. RGB Signal Amplification Section

### 7-4-1. RGB Signal Switch Circuit

The RGB input signals and the video signal demodulated into RGB signals are switched by QB011 (Analog SW: M52348FP). The block diagram of QB011 is shown in Fig. 7-4-1.




### 7-4-2. Sync Signal Process Circuit

The sync signal process circuit is applicable to the HD, VD, CS (composite sync), SYNC/G signals. HD (CS), VD and G signals developed from QB011 enter the sync separation IC (QB012: M52347FP). The sync separation priority of the sync separation IC is; HD, VD, CS and SYNC ON G in this order.

The HD and VD signals sync-separated enter the buffers QB019 and QB020 (TC7S08F) and the outputs are sent to the digital PC board.

### 7-4-3. RGB Signal Amplifier Section

The RGB signal processing section employs a wide band RGB signal IC applicable to the XGA signal. Fig. 7-4-3 shows a block diagram of QB024 (M52320SP). The control items of the IC are five items; main contrast, brightness and sub contrast for each RGB.

The brightness and main contrast controls are provided for the user adjustment, and the sub contrast are provided to equal the R, G, B levels when entering A/D converter of the digital PC board.

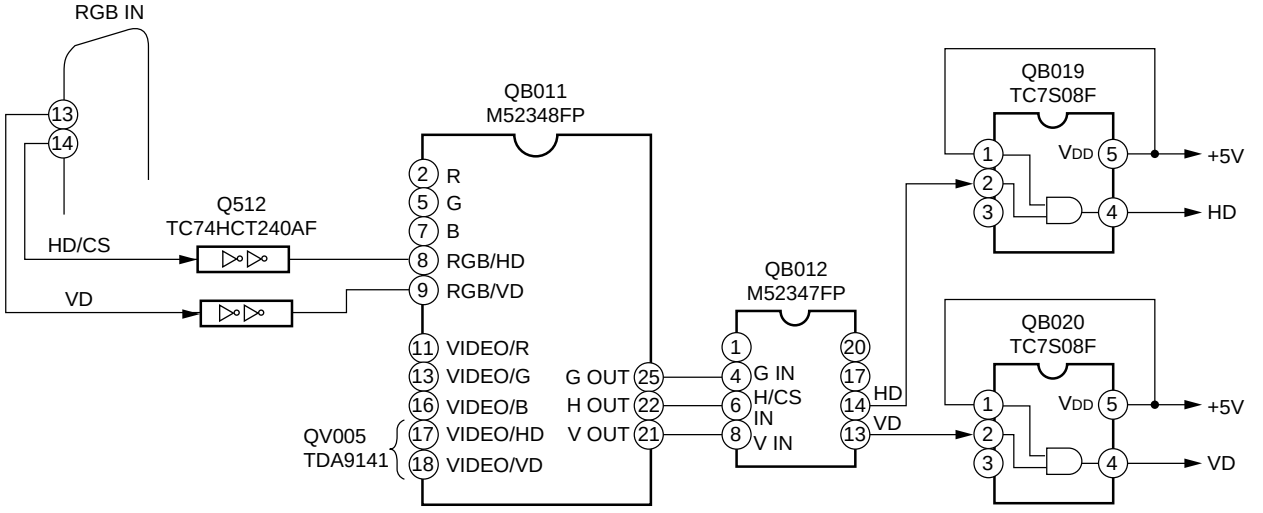



**Fig 7-4-2**

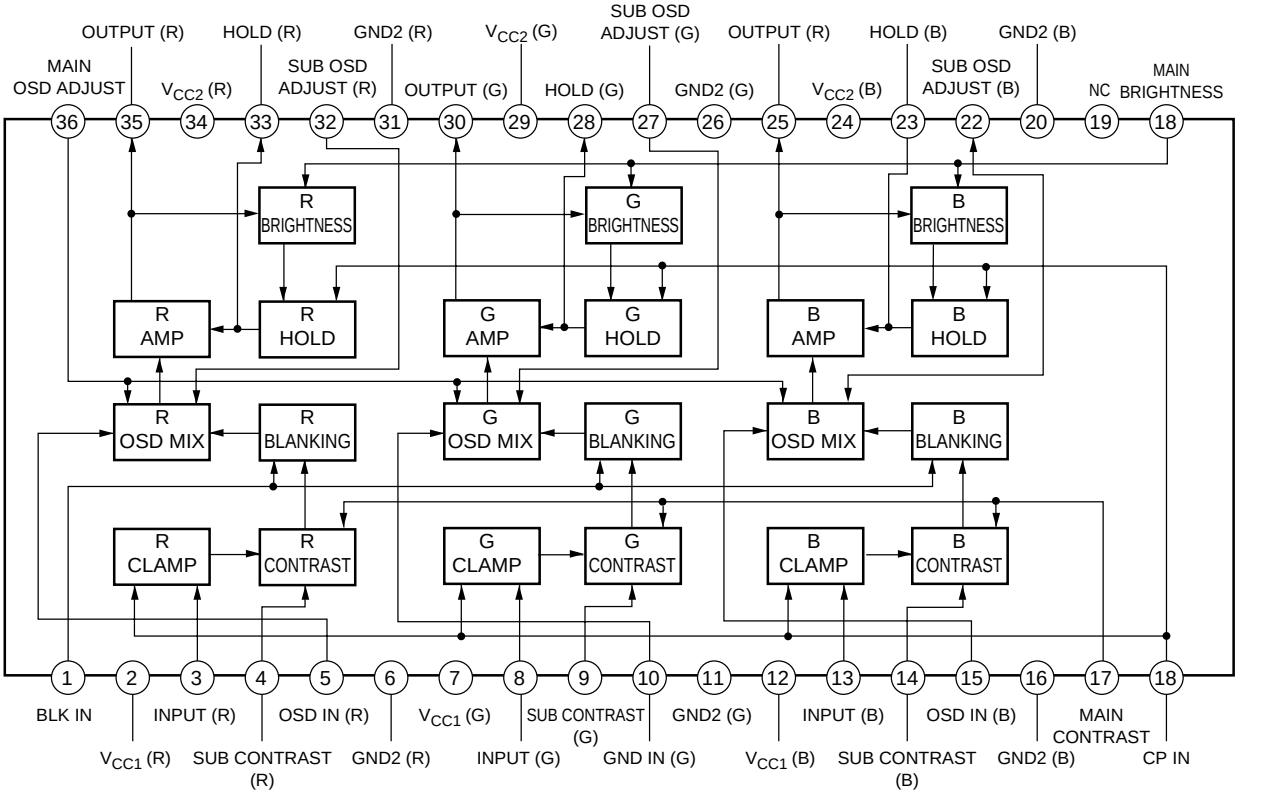



**Fig. 7-4-3**

## 7-5. Microprocessor Interface

The peripheral block diagram of the microprocessor shows in Fig. 7-5-1. All kinds of control such as signal SW, etc. are carried out by the $I^2C$ of microprocessor. The level control of RGB signal process IC (QB024: M52320SP) and the sync polarity information of the sync process IC (QB012: M52347FP) are carried out in QB025 (CXA1315M). Refer to table 7-5-1 for the logic about the polarity information of sync signal.

RGB/VIDEO SW, Audio mute/volume adjustment, etc. are controlled in QV045 (CXA1315M). Further, using camera or not, camera zoom and focus adjustment controls are carried out in QV057.

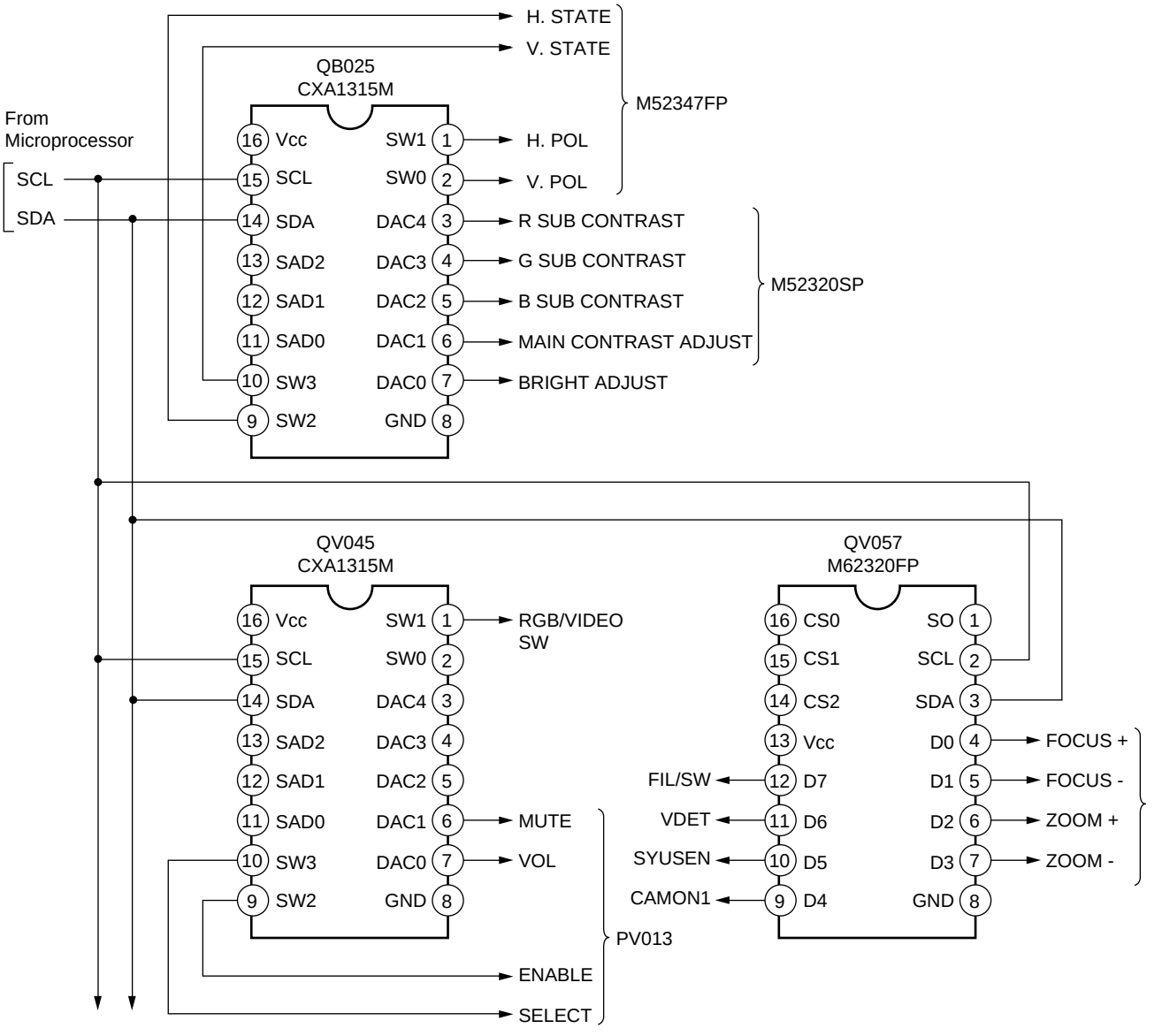



**Fig. 7-5-1**

**Table 7-5-1**

| QB012 (M52347FP) Input status | | QB025 (CXA1315M) | | | |
|---|---|---|---|---|---|
| Pin 6: HD. COMP | Pin 8: VD | SW0 (Pin 2) | SW1 (Pin 1) | SW2 (Pin 9) | SW3 (Pin 10) |
| HD. COMP. (POS.) | NON | H | H | L | H |
| HD. COMP. (POS.) | VD (POS.) | H | H | L | L |
| HD. COMP. (POS.) | VD (NEG.) | L | H | L | L |
| HD. COMP. (NEG.) | NON | H | L | L | H |
| HD. COMP. (NEG.) | VD (POS.) | H | L | L | L |
| HD. HD. COMP. (NEG.) | VD (NEG.) | L | L | L | L |
| NON | NON | H | H | H | H |
| NON | VD (POS.) | H | H | H | L |
| NON | VD (NEG.) | L | H | H | L |
| QB012 (M52347FP) output terminal | | V. POL (Pin 19) | V. POL (Pin 18) | H. STATE (Pin 1) | V. STATE (Pin 2) |

# 8. CCD CAMERA CIRCUIT (For TLP511)

## 8-1. Outline

The camera section of the unit employs the color board camera with 3 times zoom lens. The camera video circuit is assembled in one PC board and composed of the CCD and drive circuit, pre-amp and AD converting circuit (CDS, AGC and AD), video signal process circuit (DSP, MICON) and power supply circuit.

Fig. 8-1-1 shows a block diagram of CCD camera circuit.

### 8-1-1. CCD and Drive Circuit

The CCD (Q101) circuit employs 1/3 inch 480,000 pixels IT-CCD. The horizontal transmission pulse (H1, H2 and RG) and vertical transmission pulse (øV1 – øV4 and SUB) are supplied through the drive signal generation circuit and vertical drive IC (Q103 and Q202) inside DSP (Q203) by 28.5 MHz clock signal output from the oscillator (Z201).

### 8-1-2. Pre-amp and AD Coversion Circuit (CDS, AGC, AD)

The video signal developed from CCD (Q101) enters the pre-amp IC (Q201) through the buffer (Q102).

After the signal is processed the noise reduction process (CDS) inside the IC and amplified (AGC), the signal is converted to AD, and then output as 10 bits digital data.

### 8-1-3. Video Signal Process Circuit (DSP, MICON)

The video signal, which became 10 bits digital data, enters the DSP (Q203) for video signal process. After the signal is separated into the luminance and color signals, the signal process is carried out on the luminance and color signals respectively and DA-converted.

The luminance signal adds the sync signal and passes through 7 MHz low pass filter. The color signal is developed through the video driver IC (Q206) after passing 4.43 MHz band pass filter.

All kinds of parameters on DSP (Q203) are set up by the microprocessor (Q303) and picture quality adjustment, etc. are carried out.

These parameters are memorized in the $E^2$PROM (Q306). Also, the zoom, focus, etc. controls of lens are carried out by communicating with the external device through RS-232C driver IC (Q304).

### 8-1-4. Power Supply Circuit

The power supply circuit generates DC voltages (+15V, +5V, +3.3V, –8.2V) necessary to the camera signal process and power supply voltage (+9V, +5V) for lens. Lens +9V, develops the power supply voltage (+9V) entered from outside directly and for lens +5V, input +9V is developed through the regulator IC (Q801).

The signal process +5V develops the power supply voltage (+5V) entered from outside directly and the signal process +3.3V, the input +5V is developed through the regulator IC (Q802). The DC voltage of +15V, –8.2V are developed from the constant voltage circuit through the change pump circuits of Q804 – Q806.

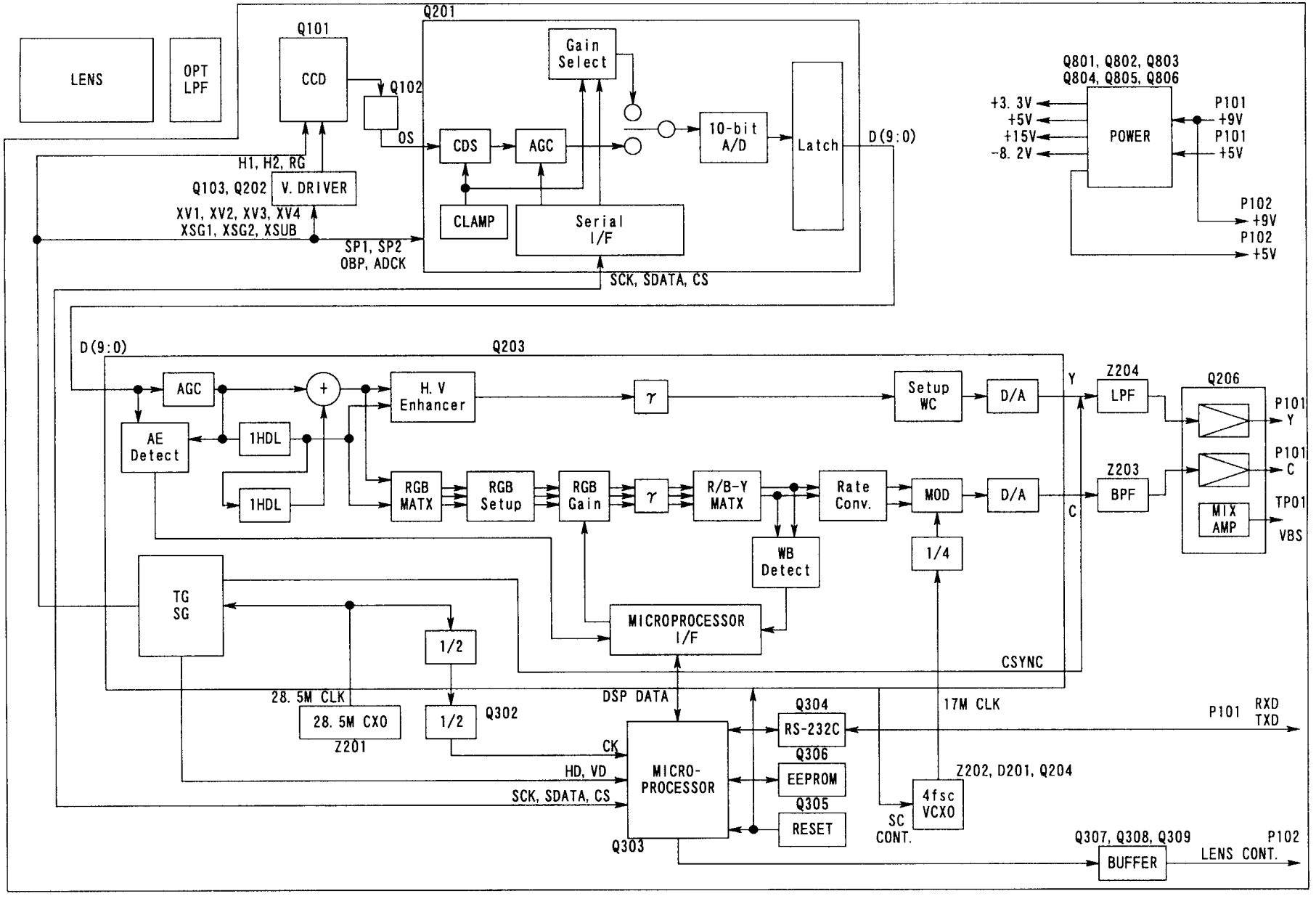



**Fig. 8-1-1 CCD camera circuit block diagram**

# 9. FLUORESCENT LAMP INVERTER CIRCUIT (For TLP511)

## 9-1. Operating Description

The base current at start-up passes through QI002, RI003, RI004, RI009 and then flows into the base of QI003. QI002 works as a ON/OFF switch for start-up operation and turns ON when the base voltage develops “L”. When the base voltage develops “H” (12V), QI002 turns off. A current flows into QI001 and RI002 only when the start-up operation is carried out, thus improves the start-up characteristics by increasing the base current of QI003. Especially, this circuit takes effective under the low temperature status where the start-up operation is likely to difficult.

DI003, DI004 and DI005 connected to QI003 base prevents an inverse break down overvoltage at QI003 $V_{BE}$. DI003 and DI004 are connected in series to prevent the overheat at short-circuiting.

When the resistor value of RI006 is small, heat generation of QI003 lowers. However, if the value is too small, the current of DI003, DI004 and DI005 in continuity becomes large.

DI002 increases only the base current of QI003 when it turns on and reduces the $V_{CE}$ (sat) of QI003 to lower the heat generation. RI005 works as a current limitation resistor of DI002.

CI004 prevents a rapid increase of the collector current of QI003 before the fluorescent lamp turns on.

Also, RI009 is a protective posistor to prevent QI003 from generating temperature more than 100°C.

The specification of LI002 is shown in Figs. 9-1-1, 9-1-2 and Table 9-1-1.

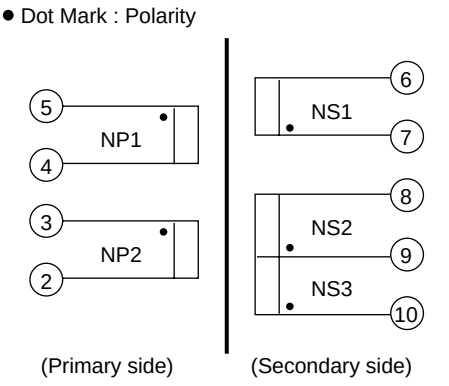



**Fig. 9-1-1 Winding specification**

**Table 9-1-1**

| No. | Coil | Terminal | Turns | Wire | Winding method |
|---|---|---|---|---|---|
| 1 | NP1 | 5 – 4 | 24 | UEW 0.3 | FIT |
| 2 | NP2 | 3 – 2 | 4 | UEW 0.2 | SPACE |
| 3 | NP2 | 9 – 8 | 144 | UEW 0.2 | FIT |
| 4 | NP3 | 10 – 9 | 10 | UEW 0.2 | FIT |
| 5 | NP1 | 7 – 6 | 10 | UEW 0.2 | FIT |

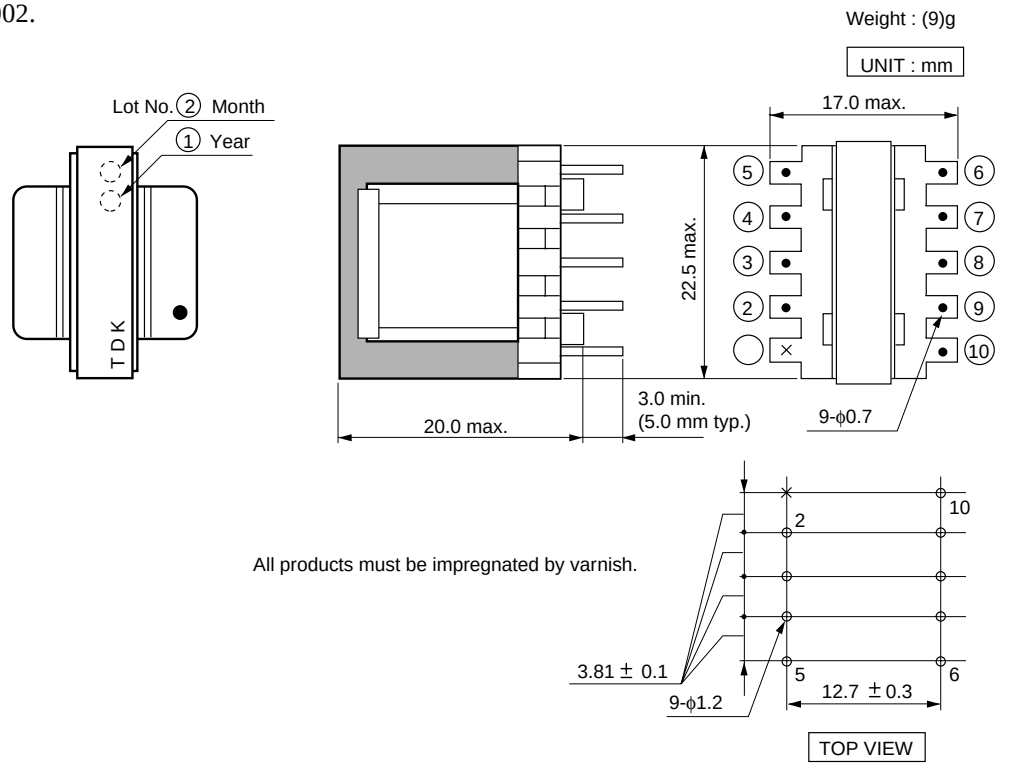



**Fig. 9-1-2 Appearance and dimensions**

CI005 and CI006 are capacitors to stabilize the fluorescent lamp discharging current. After the discharging starts, CI005 and CI006 limit the flow of the current with the reactance ($X_C = 1/wc$) of CI005 and CI006.

Before the fluorescent lamp turns on, the collector pulse of QI007 is 70 – 80 V(p-p). The voltage is stepped up to 420 – 480 V(p-p) by LI002 and applied to the fluorescent lamp. When a filament is warmed, the discharging starts and the collector voltage of QI003 becomes approx. 30 V(p-p). The fluorescent tube voltage at turning on is approx. 120 V(p-p).

ARM SW works as a ON/OFF switch for the camera power supply. When ARM SW turns on, the power is supplied to the camera.

The waveforms of each section at operation is shown in Figs. 9-1-3 and 9-1-4.

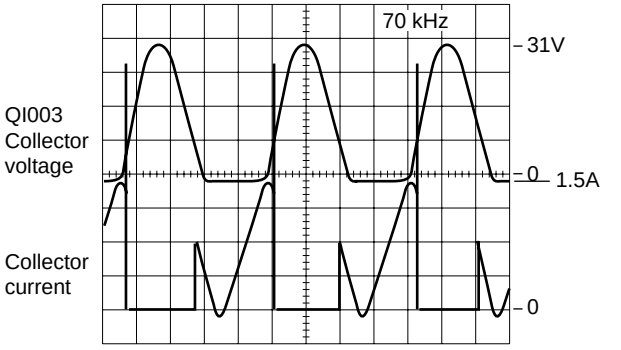



**Fig. 9-1-3**

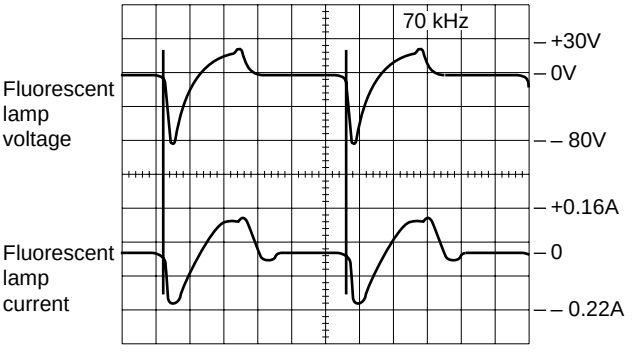



**Fig. 9-1-4**

## 9-2. Troubleshooting

### 9-2-1. Fluorescent does not turn on

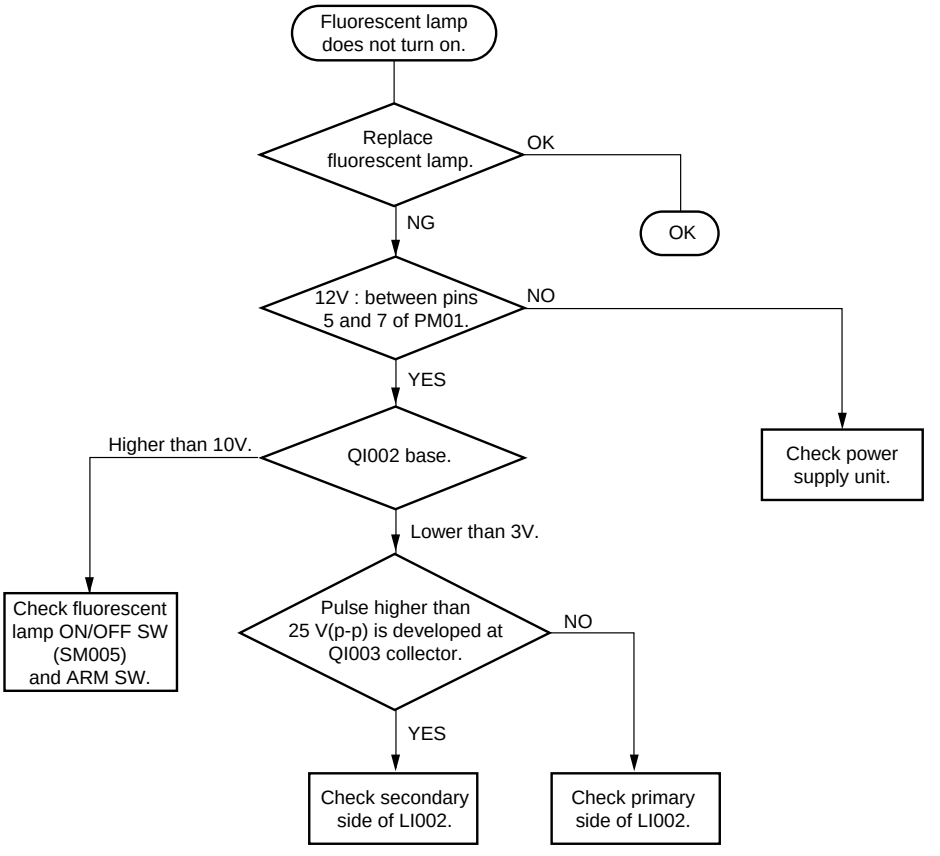



**Fig. 9-2-1**

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